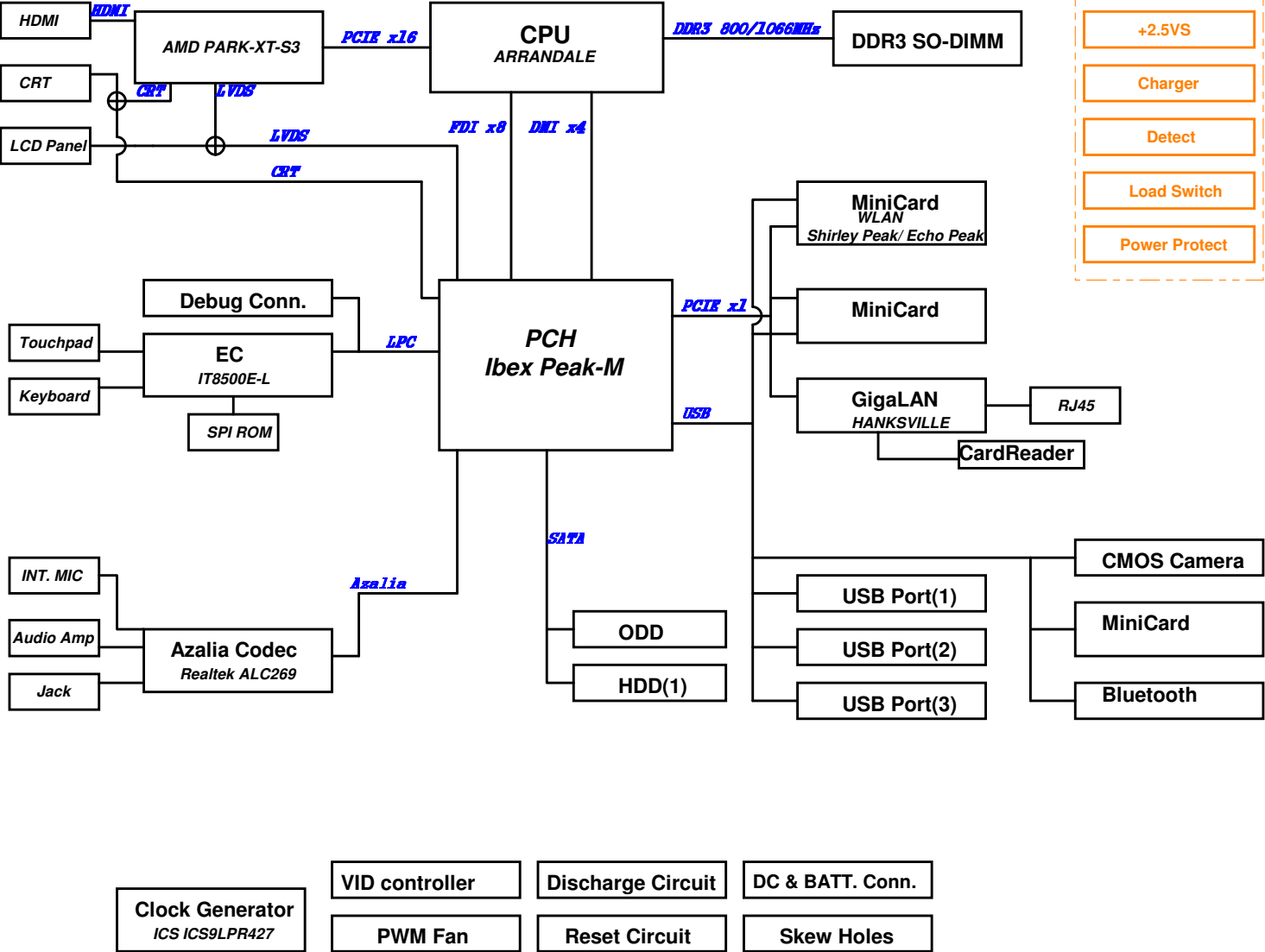


K42Jr SCHEMATIC Revision 2.0

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BLOCK DIAGRAM



Power

VCORE

System

1.5VS & 1.05VS

DDR & VTT

+2.5VS

Charger

Detect

Load Switch

Power Protect

PCH IBEX
GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAYPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	-	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSENT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	-	-	+3VS
GPIO 49	GPO	GPU_RST#	-	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	-	-	+5VS
GPIO 53	GPO	-	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	GPO	-	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	-	-	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC
IT8512

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2	-	-
GPA3	-	-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6	-	-
GPA7	-	-
GPB0	O	SUSC_EC#
GPB1	O	SUSB_EC#
GPB2	-	-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RC_IN#
GPB7	O	PM_RSMRST#
GPC0	-	-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	-	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	-	-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	-	-
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPFO	-	-
GPFI	-	-
GPFI2	I	EXP_GATE#
GPFI3	-	-
GPFI4	I	TP_CLK
GPFI5	IO	TP_DAT
GPFI6	O	THRO_CPU
GPFI7	-	-
GPFO	-	-
GPFI1	I	PM_SUSB#
GPFI2	-	-
GPFI6	-	-
GPFI0	IO	PM_CLKRUN#
GPFI1	-	-
GPFI2	O	GFX_VR_ON
GPFI3	O	BAT_LEARN
GPFI4	-	-
GPFI5	O	NUM_LED#
GPFI6	O	CAP_LED#
GPFI0	-	-
GPFI1	I	SUS_PWROK
GPFI2	I	ALL_SYSTEM_PWROK
GPFI3	I	VRM_PWROK
GPFI4	I	GFX_VR
GPFI5	I	ALS_AD
GPFI6	-	-
GPFI7	-	-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISSET_EC
GPJ4	O	TP_LED
GPJ5	-	-

EC
IT8301

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2	-	-
GPIO3	-	-
GPIO4	I	ME_+VM_PWROK
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	O	ME_PWROK
GPIO13	-	-
GPIO14	O	ME_SLP_M_EC#
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
GPIO31	-	-
GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO35	-	-
GPIO36	-	-
GPIO37	-	-

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
Clock Generator(ICS9LPR362)	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
VID Controller(ASM8272)	0011011x (36)
WiFi/WiMax	N/A
EC Master (SMB1)	
SM-Bus Device	SM-Bus Address
CPU Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

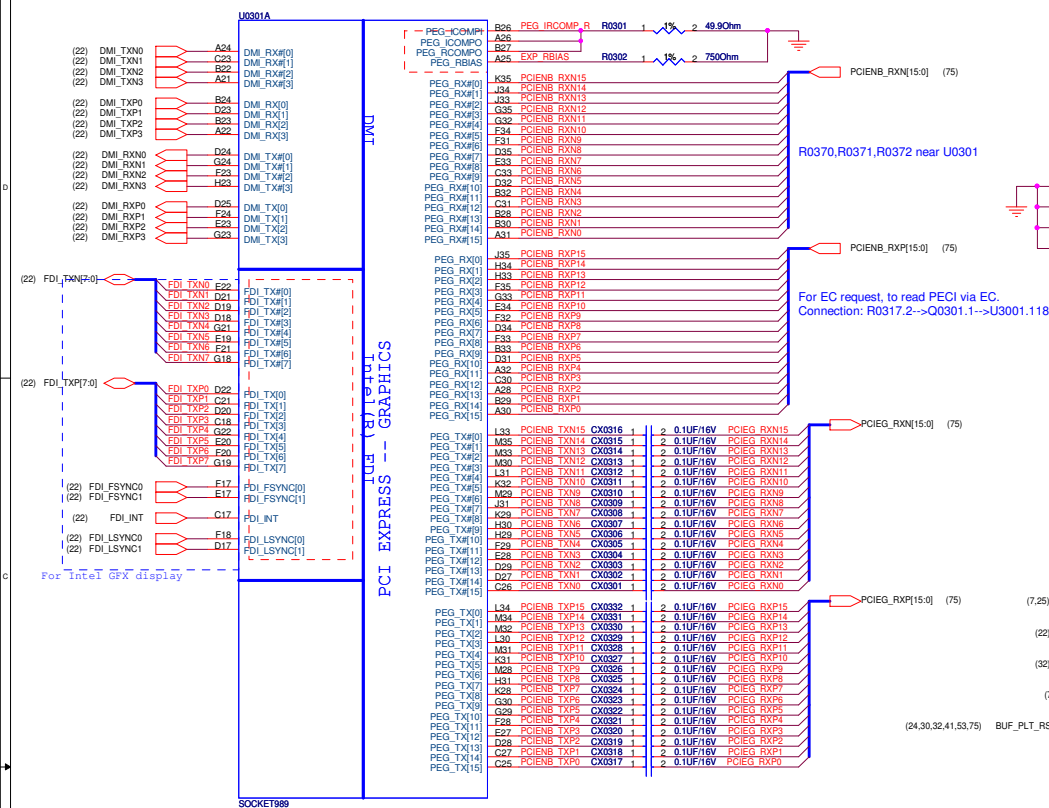
PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	ESATA (for pre-ES1)
PCIE 6	GLAN
PCIE 7	
PCIE 8	

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	NewCard
USB 6	Minicard TV Tuner
USB 7	
USB 8	
USB 9	WLAN
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

**Title : System Setting**
ASUSTek COMPUTER INC. N/A
Engineer: CH Lin

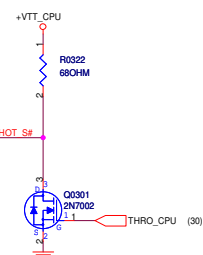
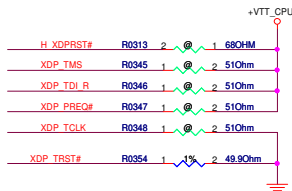
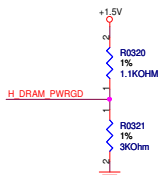
Size	Project Name	Rev
C	M60JV	1.01
Date:	Thursday, November 12, 2009	Sheet 2 of 95

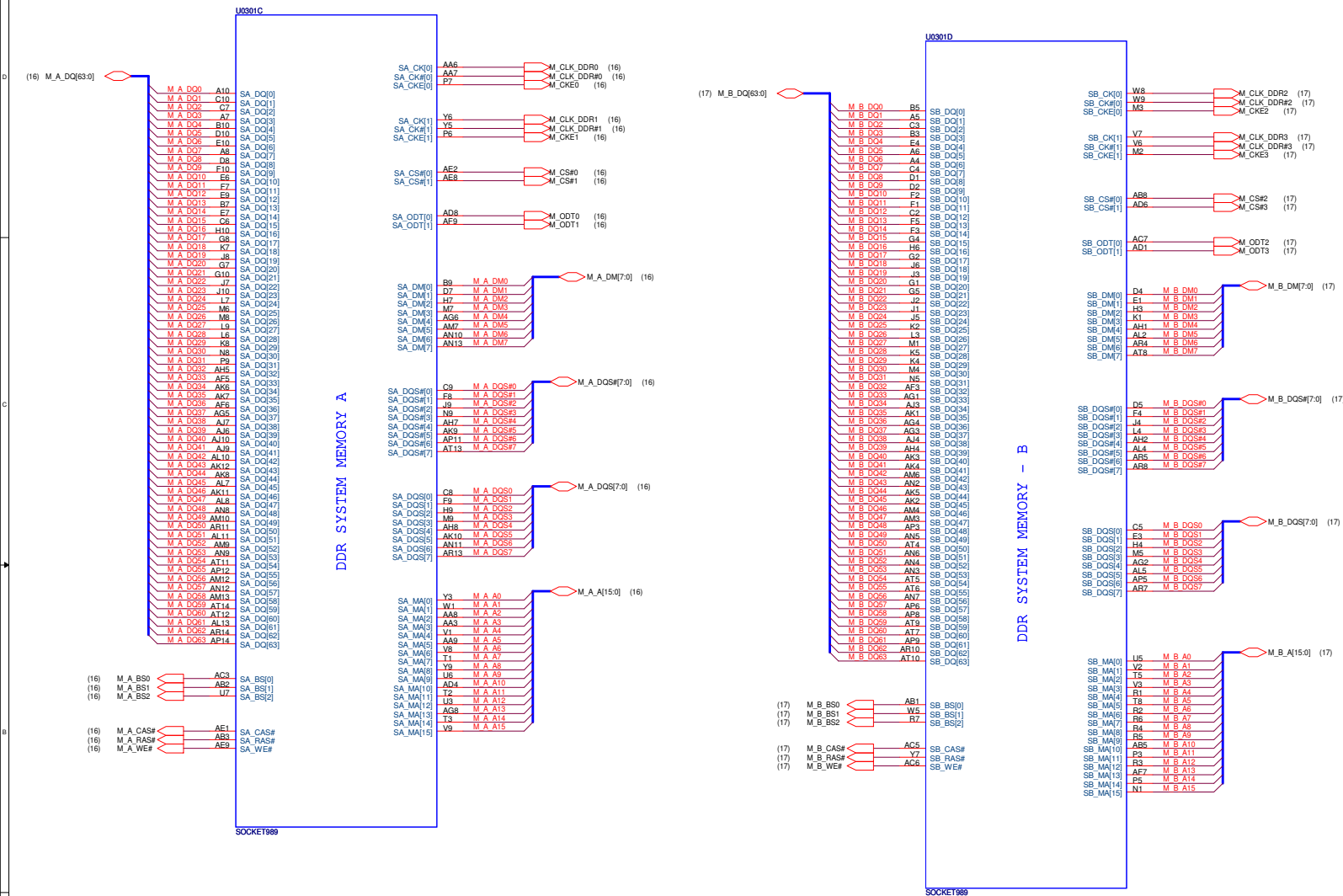


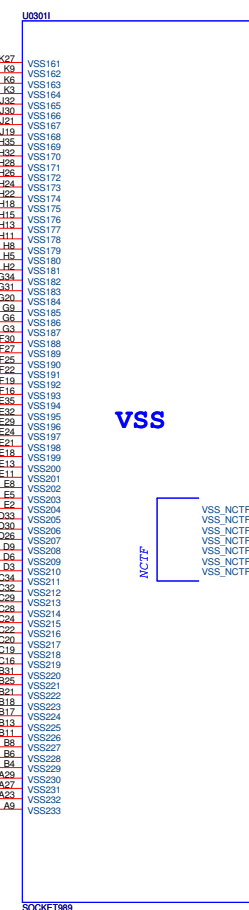
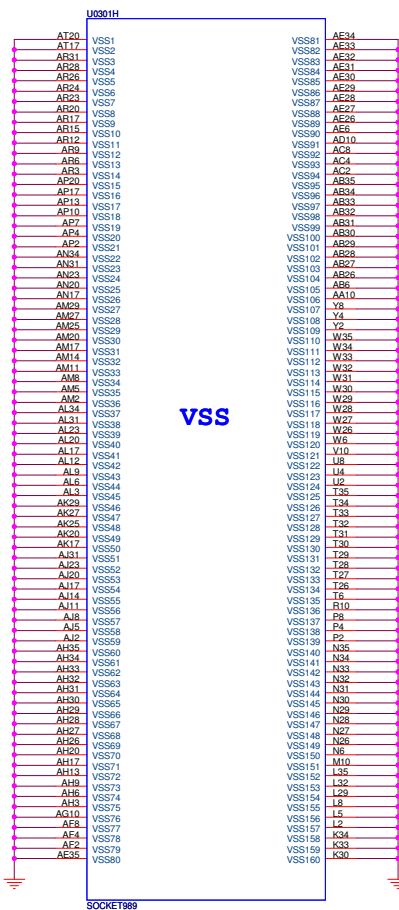
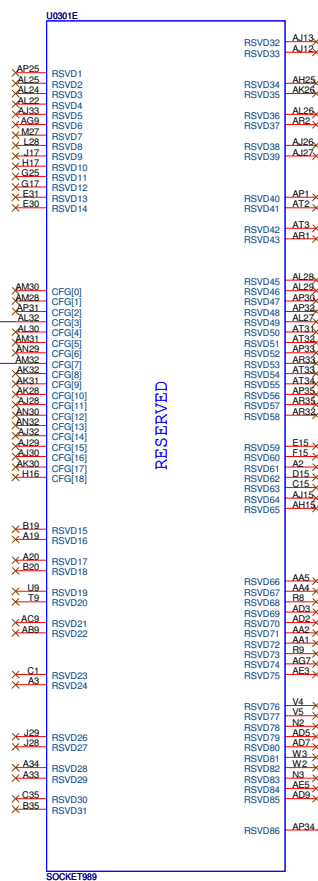
DRAMPWROK: (WW35 MoW)

Choose either one solution: --> Choose solution 2

- This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
- Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.







CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield only)

- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIe Static Numbering Lane Reversal.(Arrandale only)

- 1: Normal Operation (Default)
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale only)

- 1: Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled - An external Display Port device is connected to the Embedded Display Port

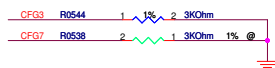
CFG[7]: Fixed for PCI Express 2.0 (latter specifications).(Clarksfield)

- 1: Connected to GND with 3.01K Ohm/5% resistor
- 0: Enabled - No pull-down resistor should be used. Does not impact Arrandale functionality.

Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.

CFG[3] - PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.

- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.

CFG[17:5] - Reserved configuration pins.

Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifurcation:

- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.

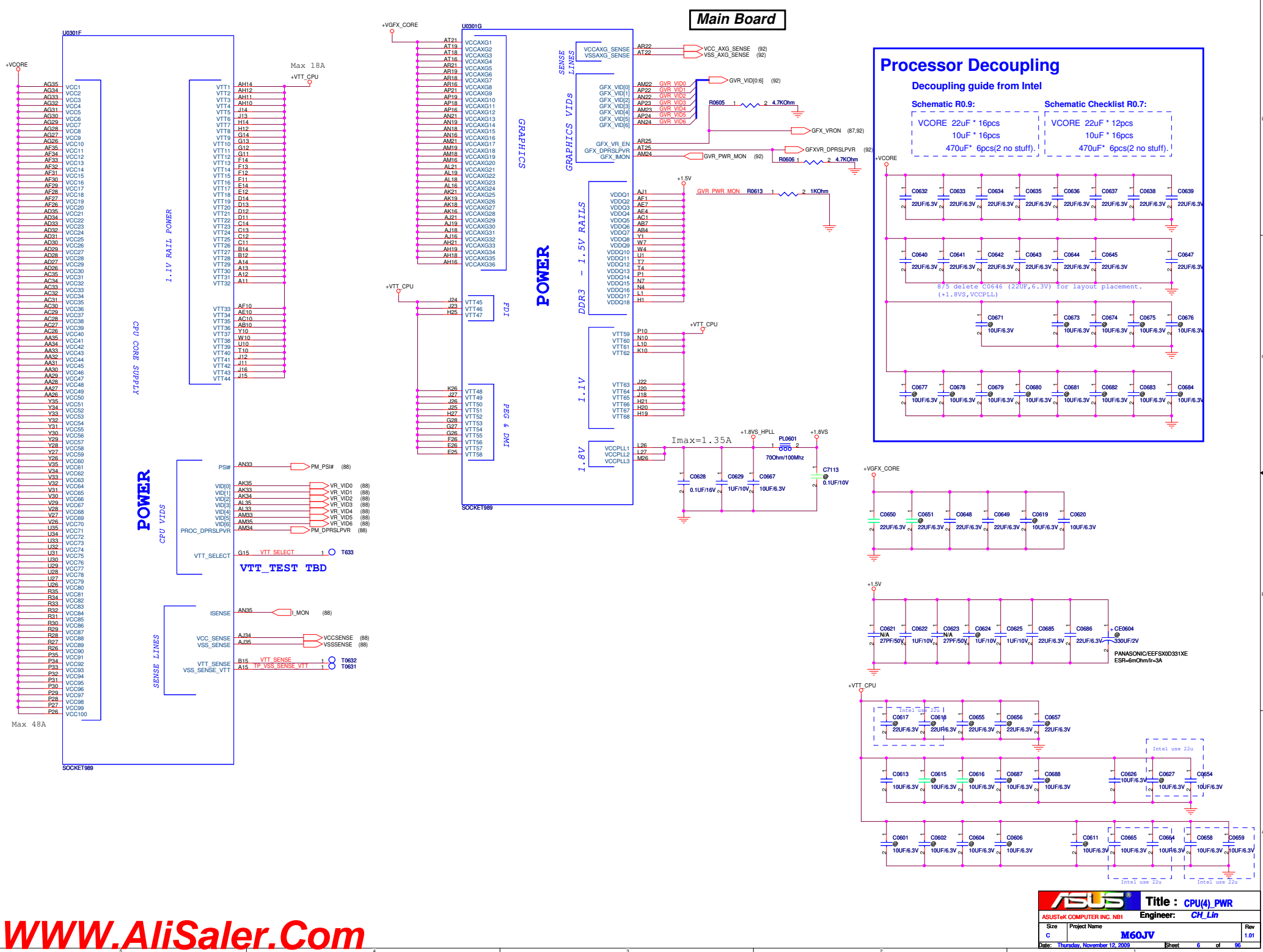
CFG[3] - Reserved (Used by Arrandale Pprocessors for PCI Express* Static Lane Numbering Reversal)

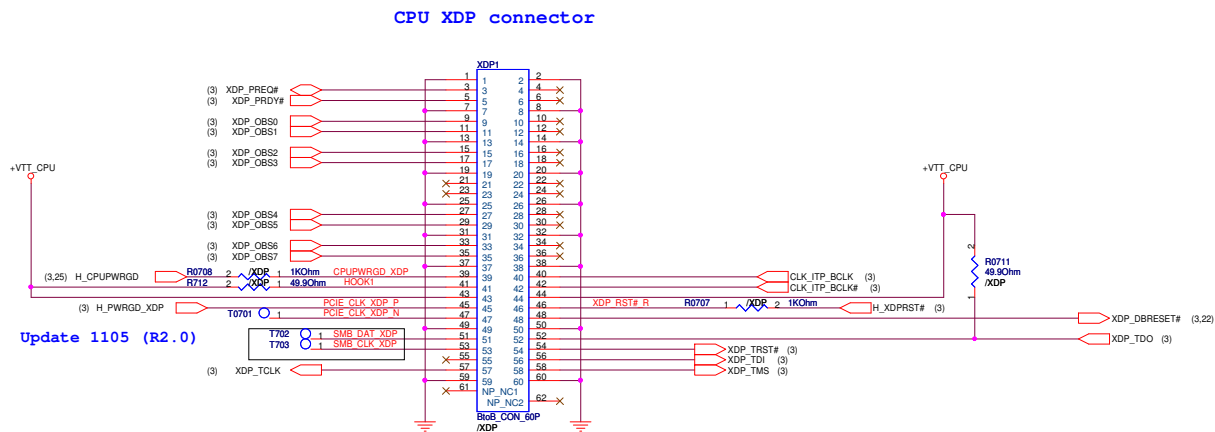
CFG[11:4] - Reserved configuration pins.

CFG[12] - N/A on Clarksfield processors.

CFG[17:13] - Reserved configuration pins.

Note: Hardware straps are sampled after RSTIN# de-assertion.





5

4

3

2

1

D

D

C


C

B

B

A

A

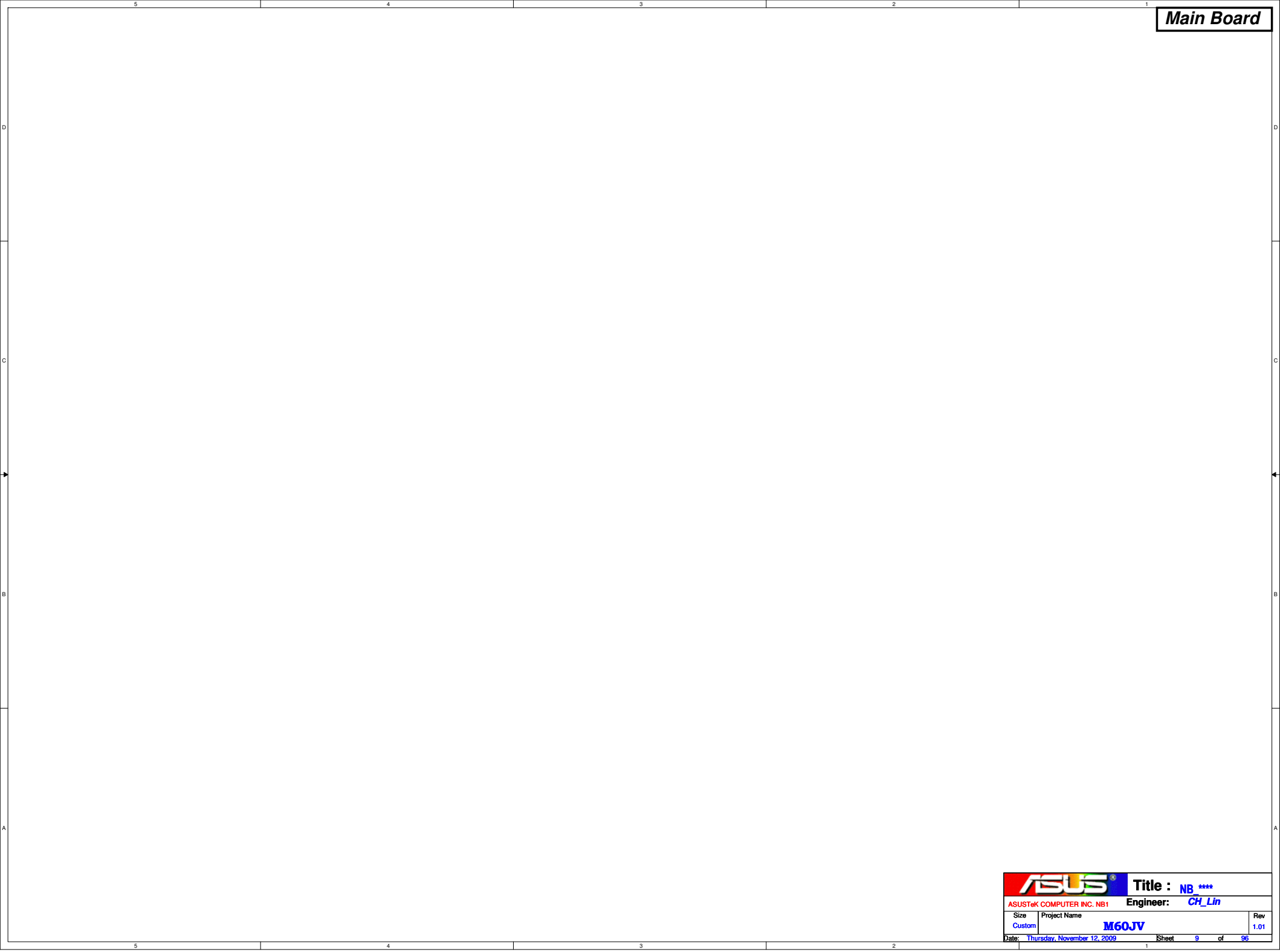


Title : NB ****

ASUSTeK COMPUTER INC. NB1Engineer: CH_Lin

Size	Project Name	Rev
Custom	M60JV	1.01

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D

D

C


C

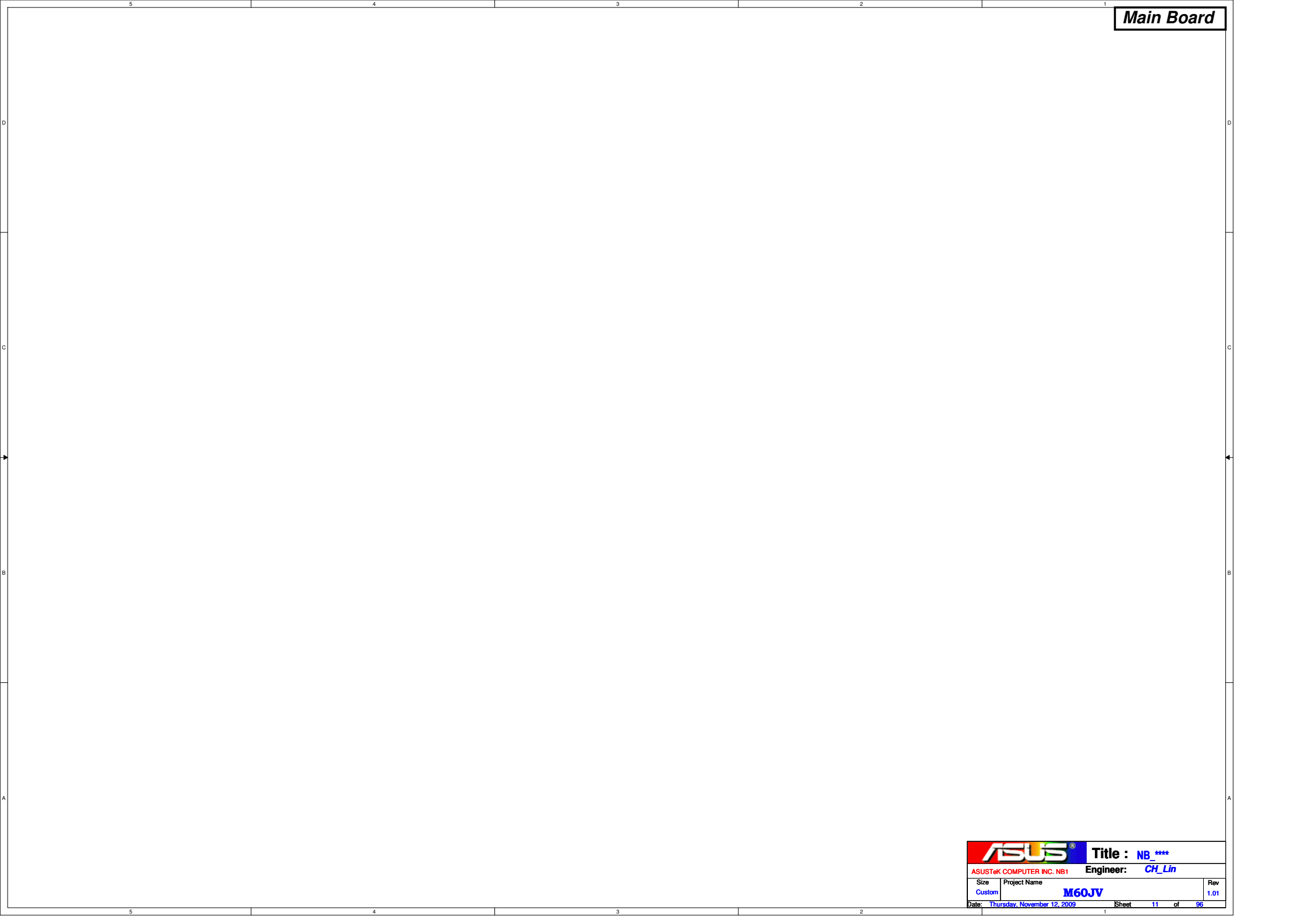
B


B

A

A

		Title : NB ****	
ASUSTeK COMPUTER INC. NB1		Engineer: CH_Lin	
Size	Project Name	Rev	
Custom	M60JV	1.01	
Date: Thursday, November 12, 2009		Sheet	10 of 96





Title : NB ****


Engineer: CH_Lin

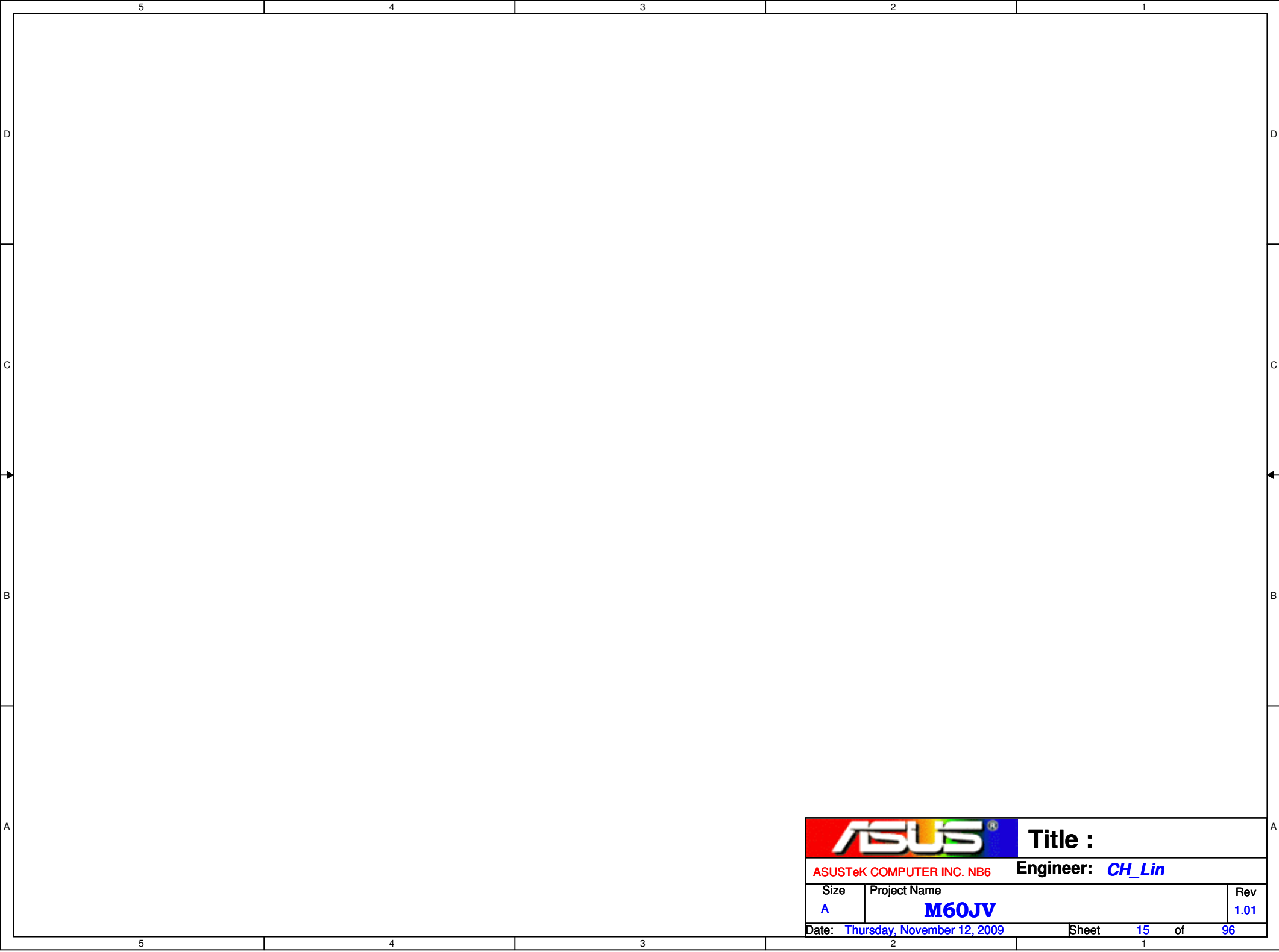
Size	Project Name	Rev
Custom	M60JV	1.01


Date: Thursday, November 12, 2009

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	5	4	3	2	1	
D						D
C						C
B						B
A						A

		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: CH_Lin	
Size A	Project Name M60JV		Rev 1.01
Date: Thursday, November 12, 2009		Sheet	14 of 96



		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>CH_Lin</i>	
Size <i>A</i>	Project Name M60JV		Rev <i>1.01</i>
Date: <i>Thursday, November 12, 2009</i>		Sheet <i>15</i> of <i>96</i>	

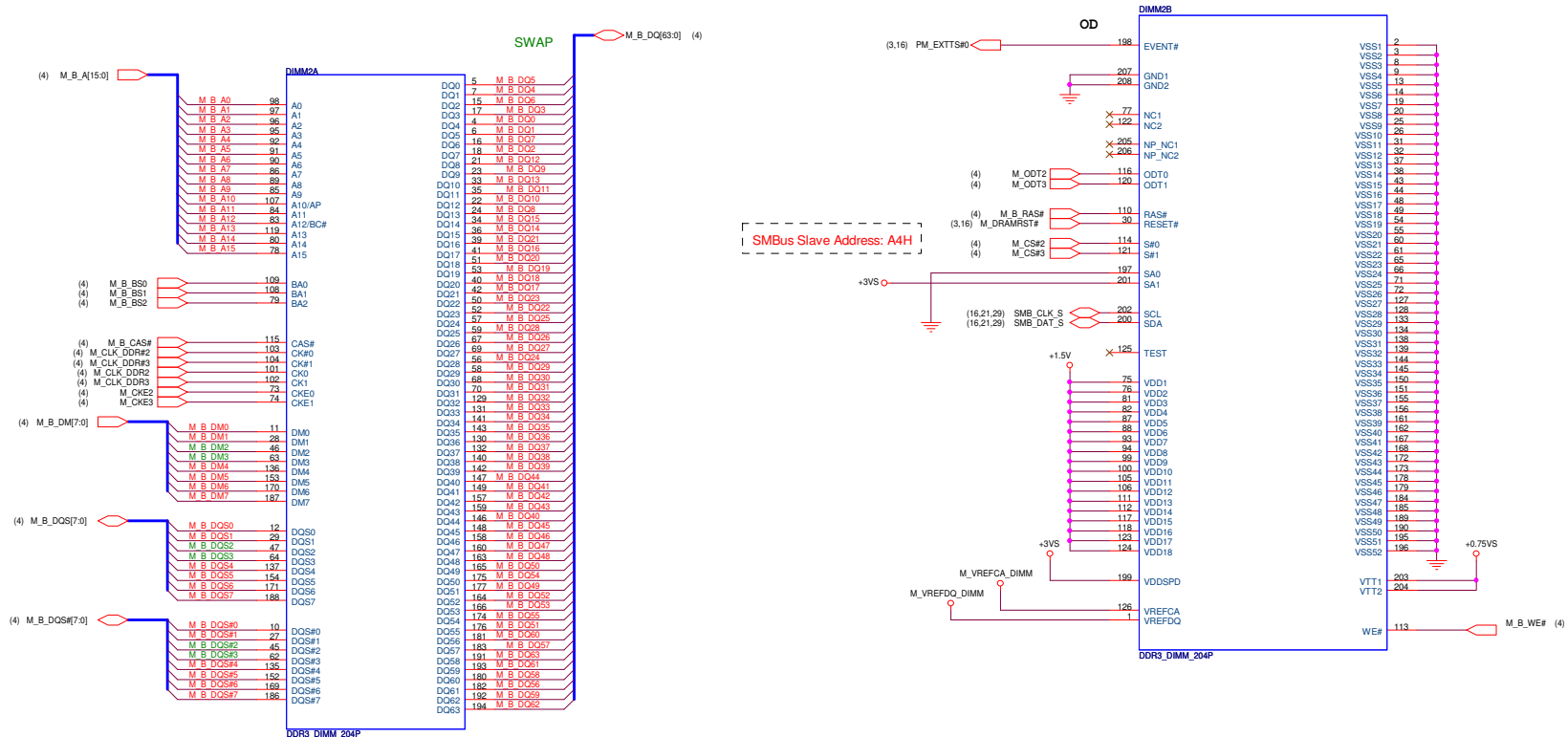


Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO_REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INT3_V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. NOTE: This signal should not be pulled low.
GNT[3]# / GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <div> <div>Bit11</div> <div>Bit 10</div> <div>Boot BIOS Destination</div> </div> <div> <div>0</div> <div>1</div> <div>Reserved</div> </div> <div> <div>1</div> <div>0</div> <div>PCI</div> </div> <div> <div>1</div> <div>1</div> <div>SPI</div> </div> <div> <div>0</div> <div>0</div> <div>LPC</div> </div> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDA TA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDA TA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDA TA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

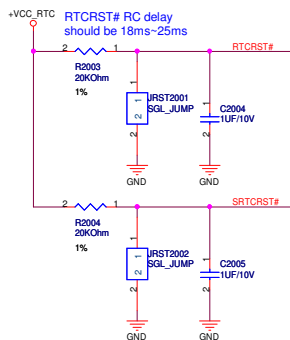
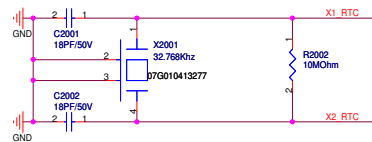
Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <div> <div>Bit11</div> <div>Bit 10</div> <div>Boot BIOS Destination</div> </div> <div> <div>0</div> <div>1</div> <div>Reserved</div> </div> <div> <div>1</div> <div>0</div> <div>PCI</div> </div> <div> <div>1</div> <div>1</div> <div>SPI</div> </div> <div> <div>0</div> <div>0</div> <div>LPC</div> </div> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GNT2# / GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. NOTE: This signal should not be pulled high

Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

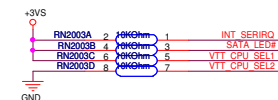
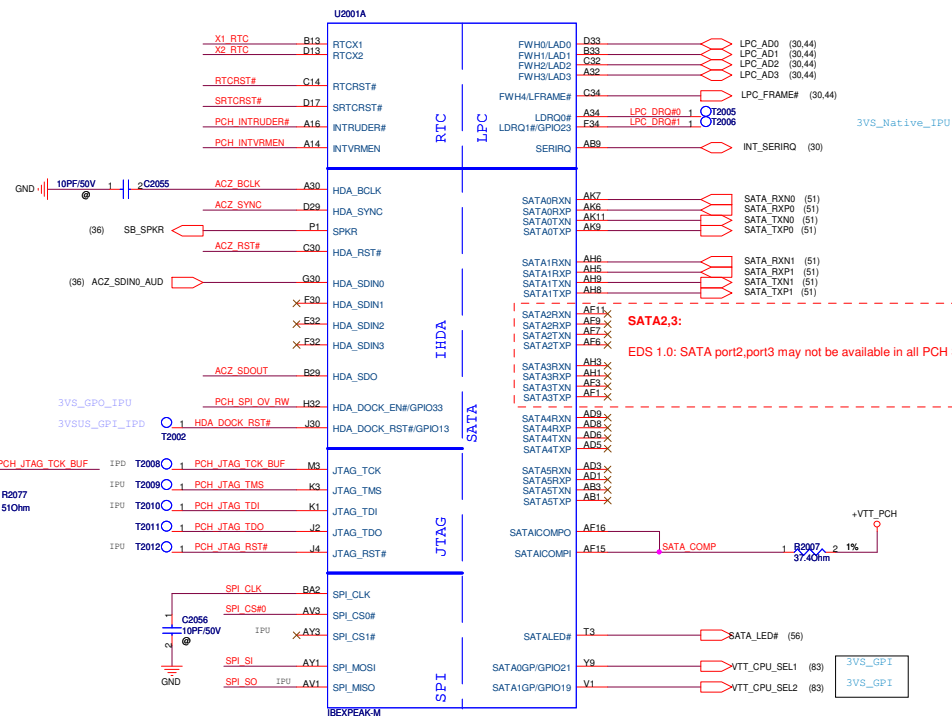
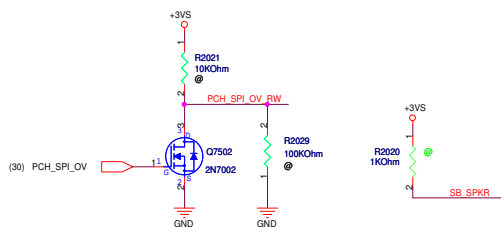
Signal	Usage	When Sampled	Comment
HDA_DOCK_EN# / GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SP1_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. NOTE: This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. NOTE: This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. NOTE: A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

<i>CMOS Settings</i>	<i>JRST2001</i>	<i>TPM Settings</i>	<i>JRST2002</i>
<i>Clear CMOS</i>	<i>Shunt</i>	<i>Clear ME RTC Registers</i>	<i>Shunt</i>
<i>Keep CMOS</i>	<i>Open (Default)</i>	<i>Keep ME RTC Registers</i>	<i>Open (Default)</i>

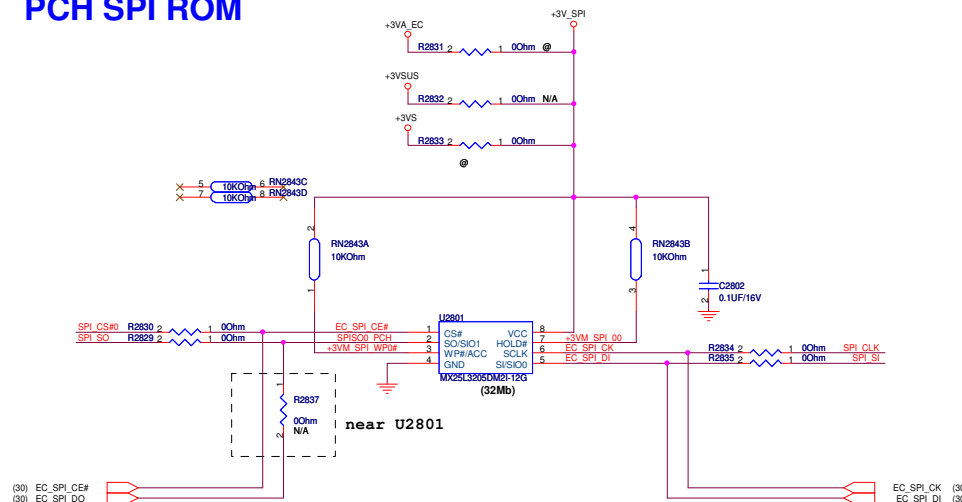


Strap information:

	H	L
ACT_SYNC: Select VCCVRRM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SFPR: No reboot strap (IPD)	No reboot	Disable No reboot
PCR_SPI_OW_RM: (IPU)	No Flash ME FW	Flash ME FW
SPI_S1: 1TPW strap. (IPD)	Enable	Disable
PCR_INTVSMEN Integrated 1.05 V VRRM Enable/Disable	Enable	Disable



PCH SPI ROM



Update 1105 (R2.0)

PCIE2: WLAN

- (S3) PCIE_RX2_WLAN
- (S3) PCIE_RXP2_WLAN
- (S3) PCIE_TX2_WLAN
- (S3) PCIE_TXP2_WLAN

PCIE5: LAN

- (41) PCIE_RX_LAN_N
- (41) PCIE_RX_LAN_P
- (41) PCIE_TX_LAN_N
- (41) PCIE_TX_LAN_P

PCIE7,8:

EDS 1.0: port7,port8 may not be available in all PCH SKUs.

3VSUS_Native_IPU

3VS_Native

- (S3) CLK_PCIE_WLAN# PCH
- (S3) CLK_PCIE_WLAN_PCH
- (S3) CLKREQ2_WLAN#

WLAN do not support

CLK REQ3#

CLK REQ4#

CLK REQ5#

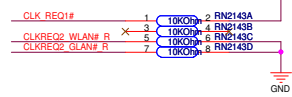
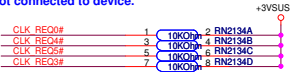
- (41) PCH_C_LAN_N
- (41) PCH_C_LAN_P

- (41) CLKREQ2_GLAN#

Imc251 do not support

Note: Place these
resistors near
to PCIe Slots

PCH CLKREQ Setting:
Not connected to device.



U2001B

PCI-E**

Controller

Link

From CLK BUFFER

Clock Flex

SMBALERT#/GPIO11

SMBCLK

SMBDATA

SML0ALERT#/GPIO60

SML0CLK

SML0DATA

SML1ALERT#/GPIO74

SML1CLK/GPIO58

SML1DATA/GPIO75

CL_CLK1

CL_DATA1

CL_RST1#

PEG_A_CLKREQ#/GPIO47

CLKOUT_PEG_A_N

CLKOUT_PEG_A_P

CLKOUT_DMI_N

CLKOUT_DMI_P

CLKOUT_DP_N/CLKOUT_BCLK1_N

CLKOUT_DP_P/CLKOUT_BCLK1_P

CLKIN_DMI_N

CLKIN_DMI_P

CLKIN_BCLK_N

CLKIN_BCLK_P

CLKIN_DOT_96N

CLKIN_DOT_96P

CLKIN_SATA_N/CLKIN_SATA_P/CLKIN_SATA_P/CLKIN_SATA_P

REFCLK14N

CLKIN_POILOOPBACK

XTAL25_IN

XTAL25_OUT

XCLK_RC0MP

CLKOUTFLEX0/GPIO64

CLKOUTFLEX1/GPIO65

CLKOUTFLEX2/GPIO66

CLKOUTFLEX3/GPIO67

PEG_B_CLKREQ#/GPIO56

IBEXPEAK-M

B9

H14

C8

J14

C6

G8

M14

E10

G12

T13

T11

T9

H1

AD43

AD45

AN4

AN2

AT1

AT3

AW24

BA24

AP3

AP1

F18

E18

AH13

AH12

P41

J42

AH51

AH53

AF38

T45

P43

T42

N50

EC_SCI# (22,30)

PCH SMBCLK

PCH SMBDATA

WLAN_ON (S3)

SML0_CLK

SML0_DAT

BT_ON (61)

SML1_CLK

SML1_DAT

DG2.0 P241

When unused, CL_CLK1, CL_DATA1 and CL_RST1# may be left unconnected.

3VSUS_Native

PARK_PECCLK_REQ# (72,75)

CLK_PCIE_PEG_PCH

CLK_PCIE_PEG_PCH

CLK_DMI_PCH (3)

CLK_DMI_PCH (3)

CLK_DREF# EDP

CLK_DREF# EDP

C_PCH_DMI# (29)

C_PCH_DMI# (29)

C_PCH_BCLK# (29)

C_PCH_BCLK# (29)

C_96M_DOT# (29)

C_96M_DOT# (29)

C_PCH_SATA# (29)

C_PCH_SATA# (29)

C_14M_PCH (29)

CLK_PCIE_FB (24)

3VS_Native_IPD

3VS_Native_IPD

3VS_Native_IPD

3VS_Native_IPD

3VS_Native_IPD

3VS_Native_IPD

3VS_Native_IPD

If not use crystal, please change C1201 to 0 08M

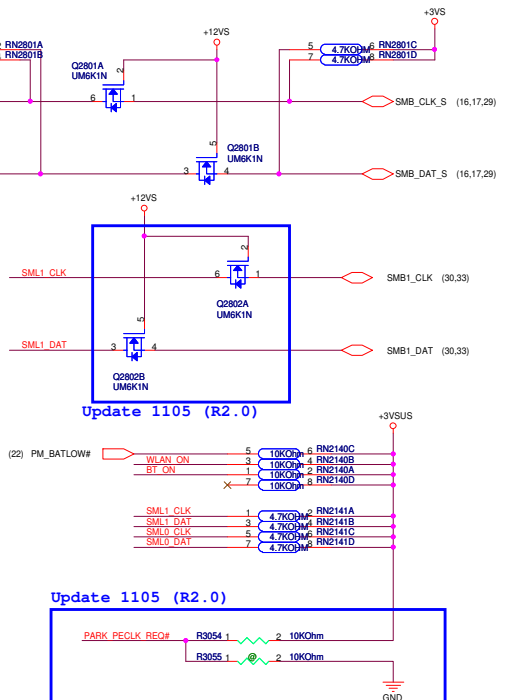
R2120: For Xtal measurement

DG2.0

Section 4.2.4.1: Added 25-MHz Crystal routing guideline. All Mobile Intel 5 Series Chipset-based Integrated Graphics platforms are required to use a 25-MHz crystal on the PCH XTAL25_IN/OUT to enable the PCH to generate the display clocks. Display clock generation is integrated into the PCH.

Integrated Graphics platforms that implement DVI/DP/HDMI/e-DP are required to use Display Clock Integration (DCI) (25M crystal to generate PCH display clocks) to improve signal integrity and mitigate risk of electrical compliance and associated functional failures

WW35 Update: Integrated Graphics platforms that use only LVDS and/or VGA Displays may use Buffer Through Mode (BTM) and leave 25-MHz crystal and RC components unstuffed



Update 1105 (R2.0)

Update 1105 (R2.0)

C_14M_PCH C7764 2

CLK_PCIE_FB C7765 2

10PF/50V

10PF/50V

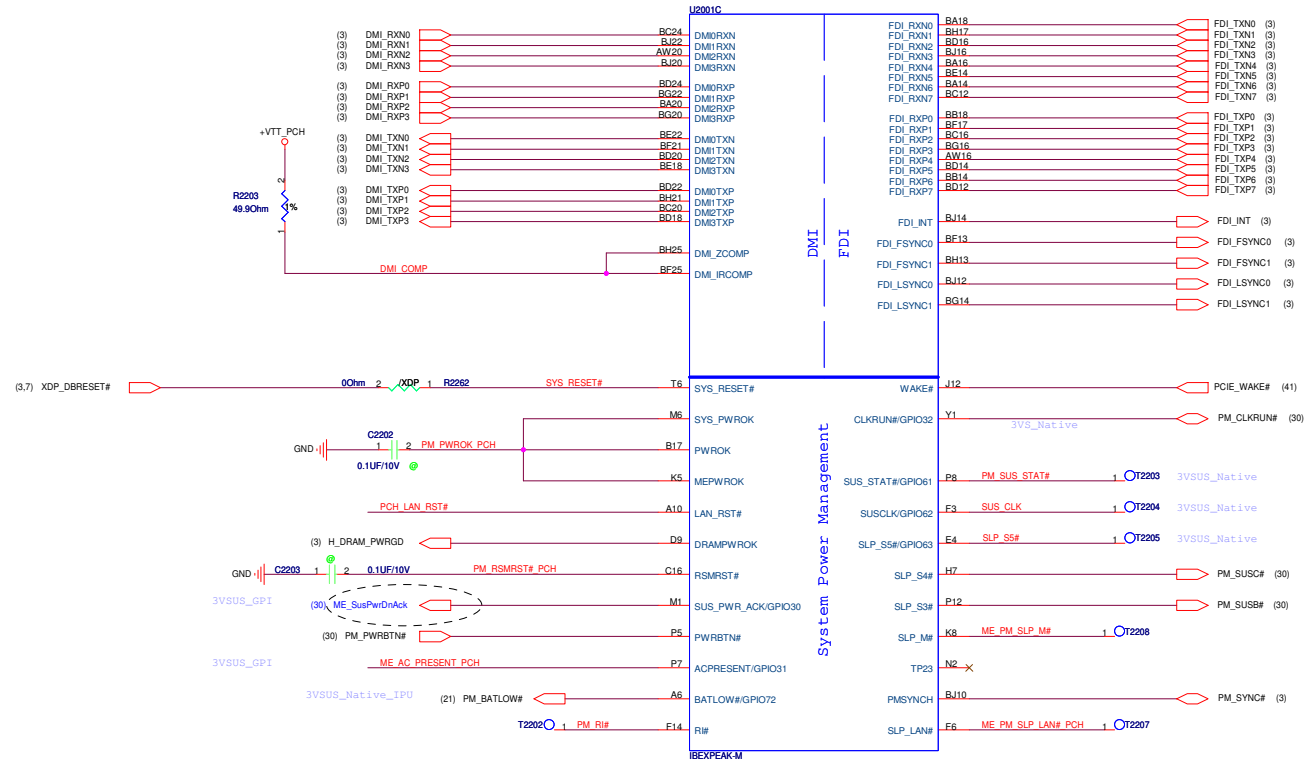
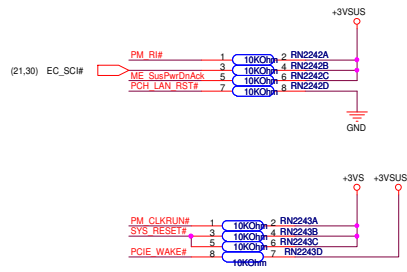


Title : PCH_IBEX(2)_PCE,CLK,SMB,PEG

Engineer: James1_Wu

Size	Project Name	Rev
C	M52J	1.01
Date:	Thursday, November 12, 2009	Sheet 21 of 95

```
pre-ES1 not support
Reversal Feature
```



R1.1,item L15

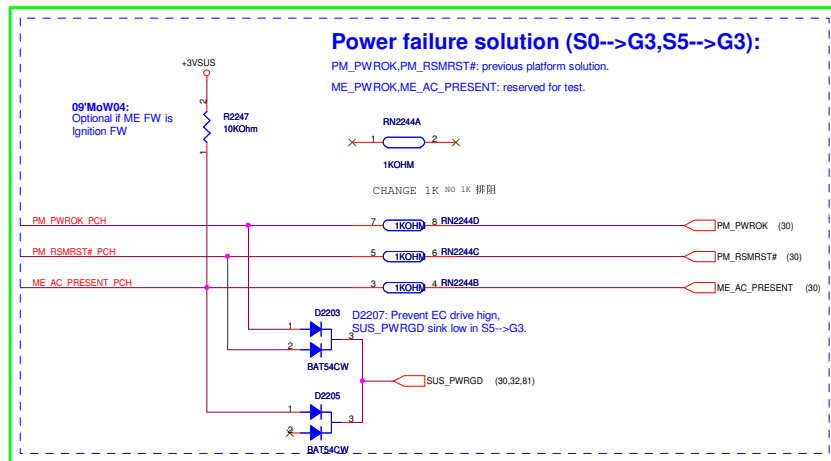


Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required Note: Optional if Intel ME Firmware is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required Note: If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel® ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.



1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:
VccALVDS, VccTX LVDS



- 1. NC:**
CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYCN,CRT_VSYNC
- 2. 1-k Ω \pm 0.5% pull-down to GND:**
DAC_IREF
- 3. Connected to GND:**
CRT_ITRN
- 4. Connect to +V3.3:**
VCCADAC

DGPU_SELECT#:
0=GPU, 1=GPU

PCI_PME#: Internal PU to suspend plane.
change to PCI_CLK4 to sync ICS364

GNT0#,GNT1#: Boot BIOS Strap.

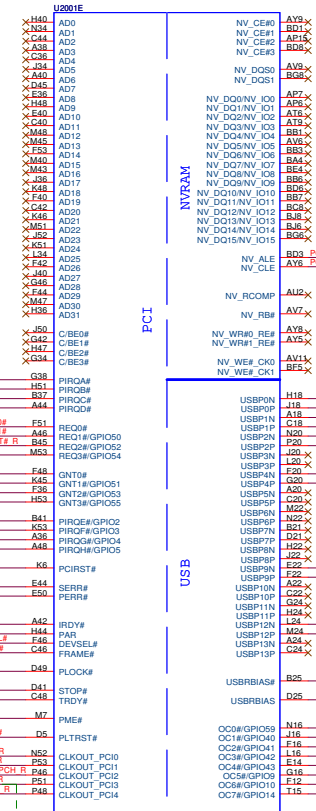
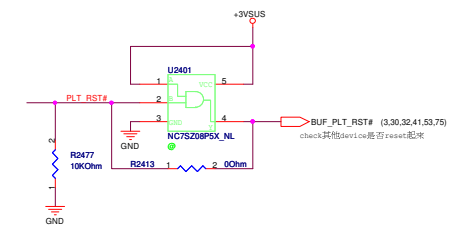
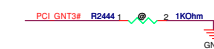
Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

Sampled on rising edge of PWROK.



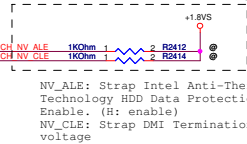
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default



Strap information:

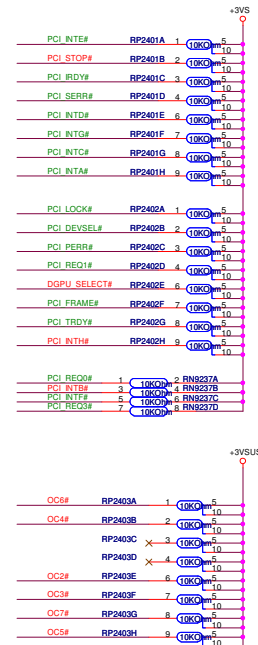
	H	L
PCU_NV_ALE: Strap Intel Anti-Theft Technology HDD Data Protection Enable	Enable	Disable
NV_CLE: Strap DMI Termination voltage		

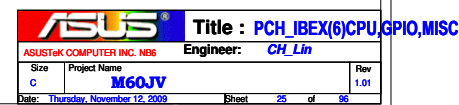
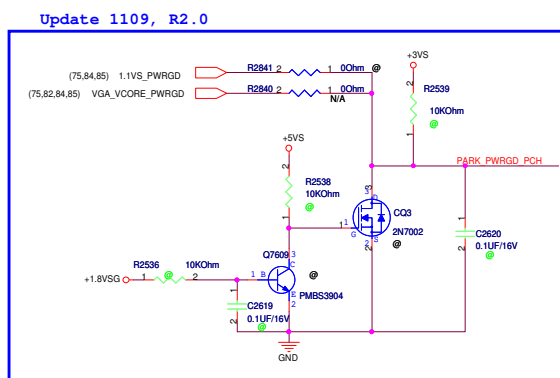
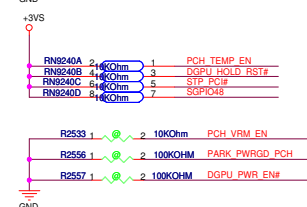
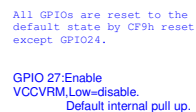


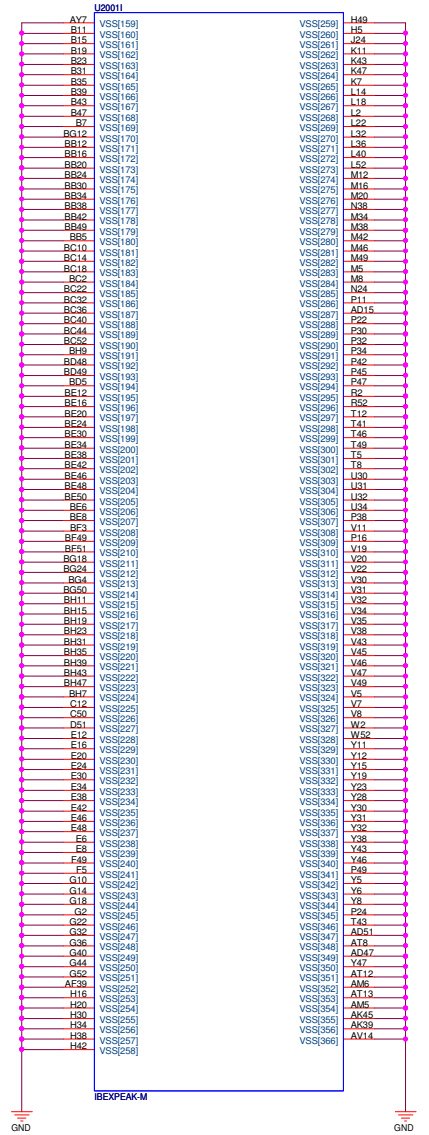
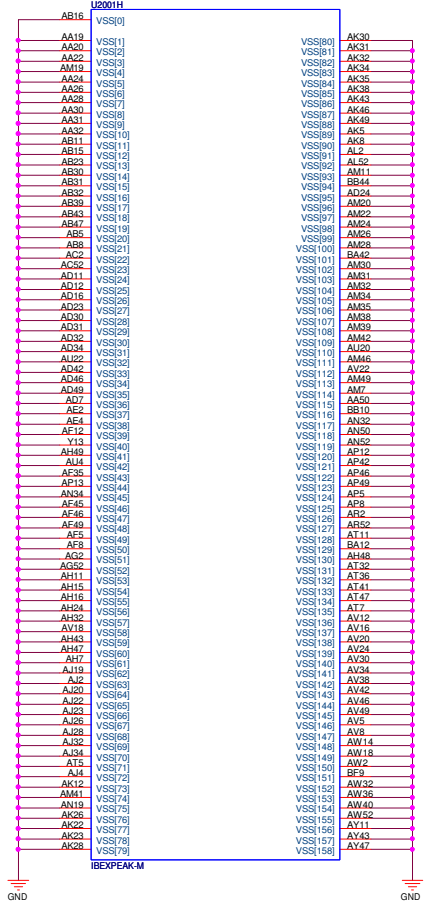
NV_ALE: Strap Intel Anti-Theft Technology HDD Data Protection Enable. (H: enable)
NV_CLE: Strap DMI Termination voltage

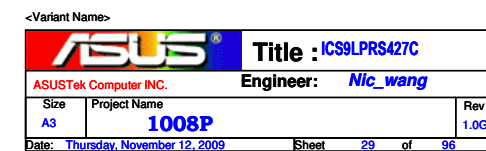
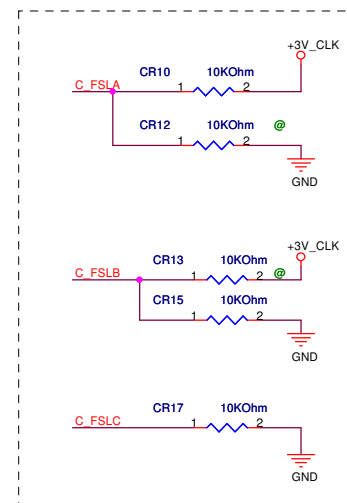
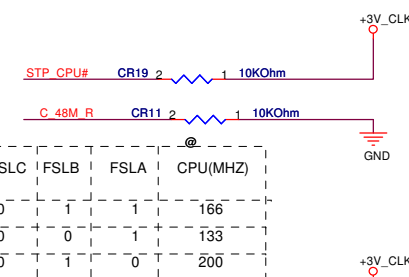
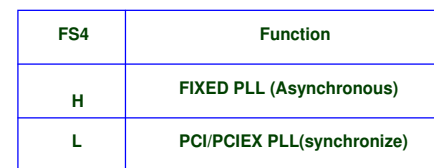
K82JR	Recommend settings
0 USB port	
1 USB port	
2 USB port	
3	
4 WiFi/WiMax	
5	
6	
7	
8	
9 Camera	
10	
11	
12 BT (1.1)	
13	

3VSUS_Native [9,10,14,40,41,42,43,59]



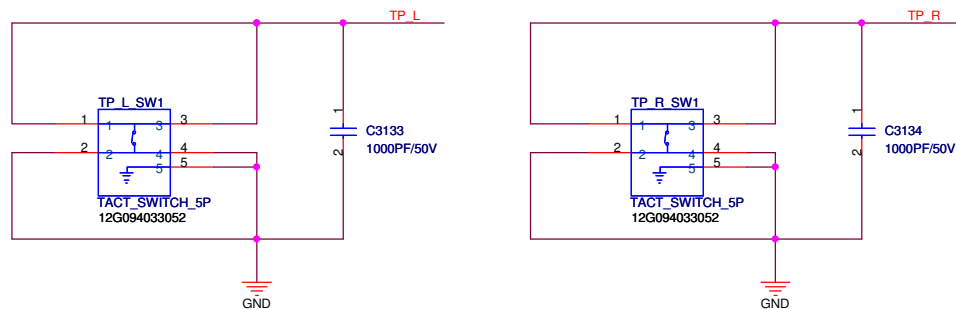




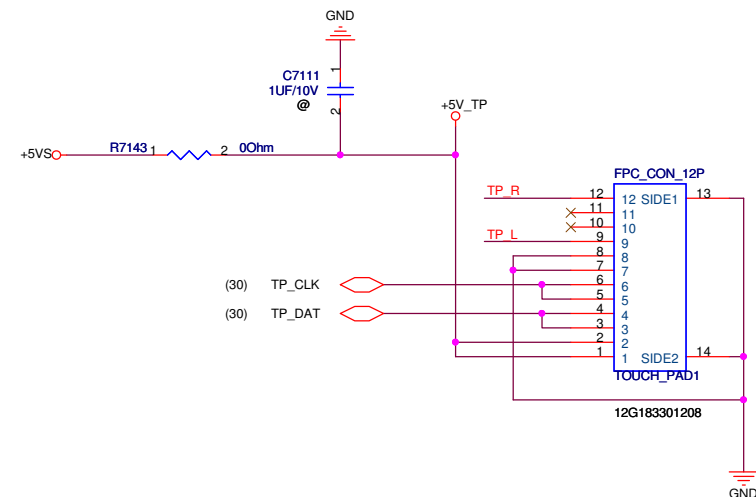




TouchPad

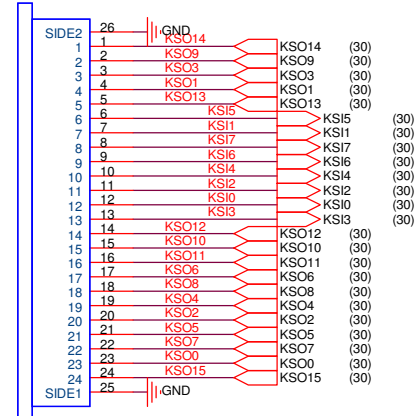


1.0 EMI test need mount C3133 and C3134



Keyboard Connector

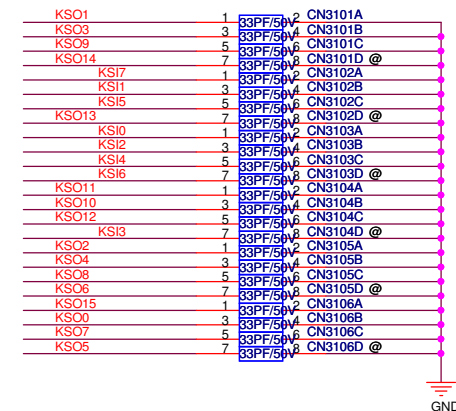
KB_CON1



FPC_CON_24P

12G182102402

EMI Request



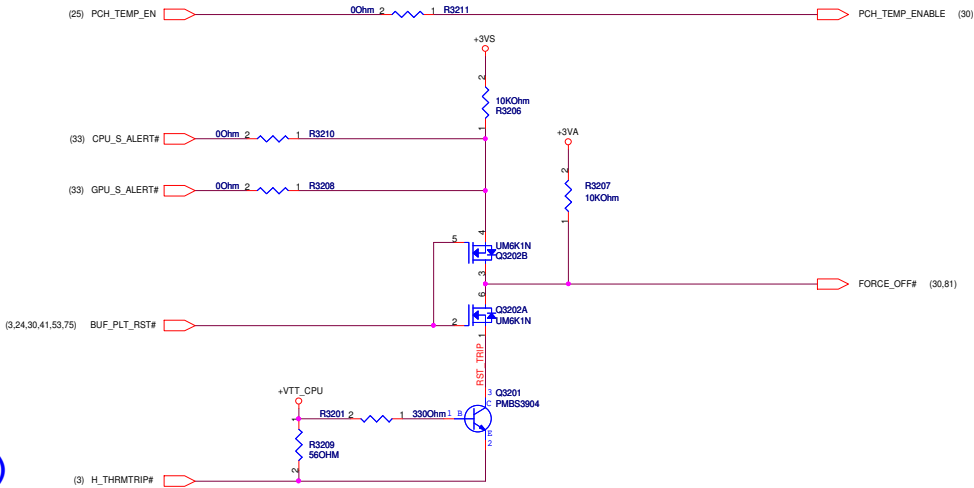
<Variant Name>

Thermal Policy

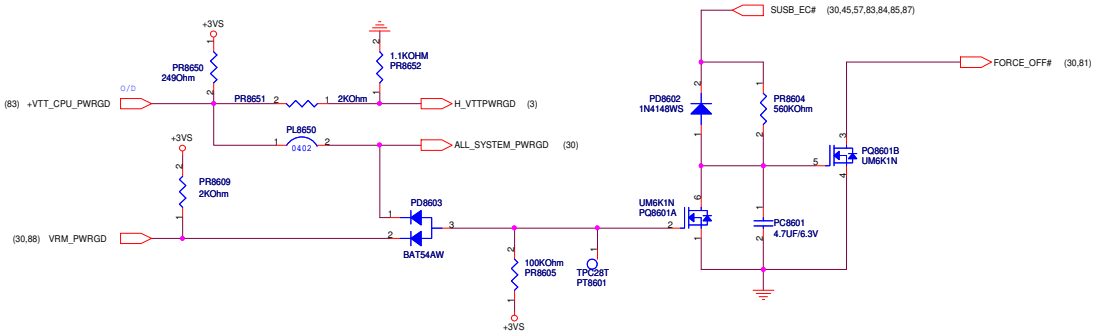
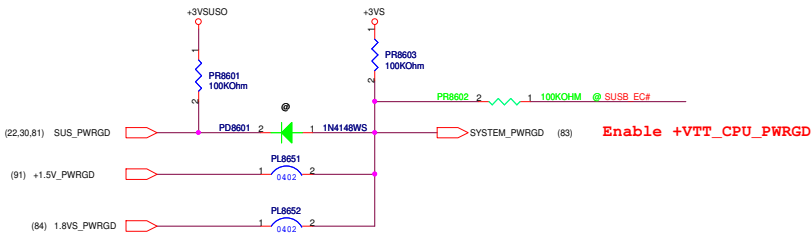
Input 1(sensor)

Input 2(thermtrip)

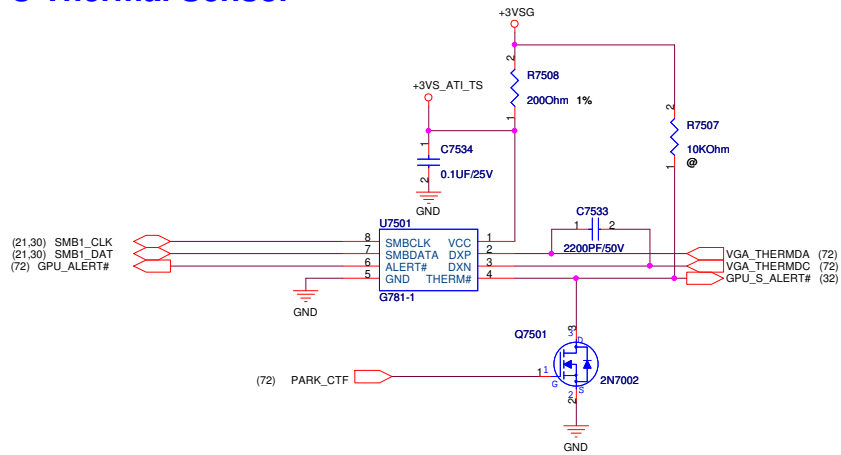
Output (shut down)



POWER GOOD DETECTER

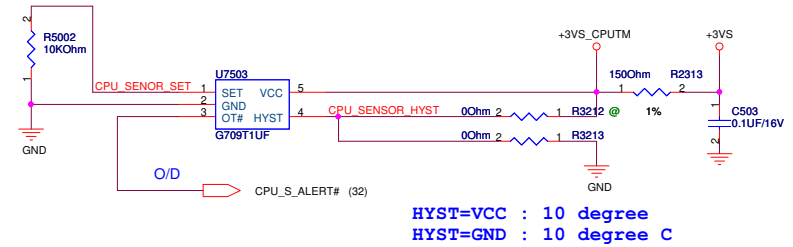


GPU Thermal Sensor



CPU Thermal Sensor

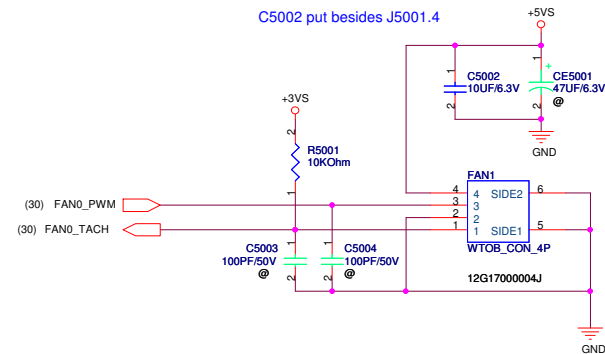
Update 1108 (R2.0)



U7503 under CPU socket

PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.

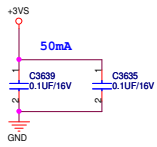


ASUS		Title : AR8131	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	LAN Design IP	108	
Date: Thursday, November 12, 2009		Sheet 33 of 96	

移至 USB BOARD

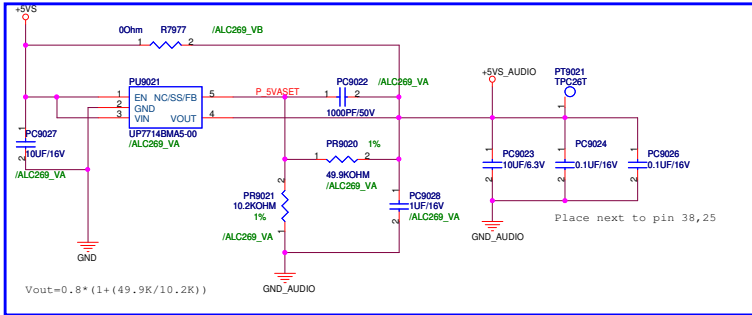
<Variant Name>

		Title : 8131	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	LAN Design IP		108
Date: Thursday, November 12, 2009		Sheet	34 of 96



Close to pin1,9

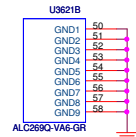
Update 11.08 (R2.0)



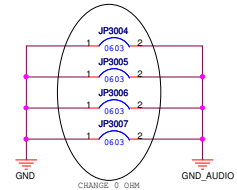
$$V_{out} = 0.8 \times (1 + (49.9K / 10.2K))$$



Place next to pin 39,46

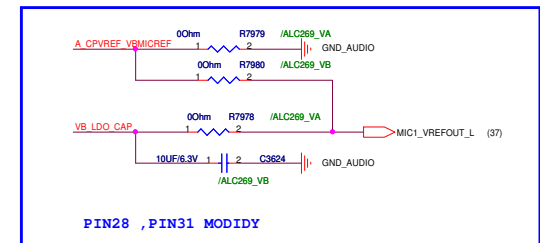


For EMI

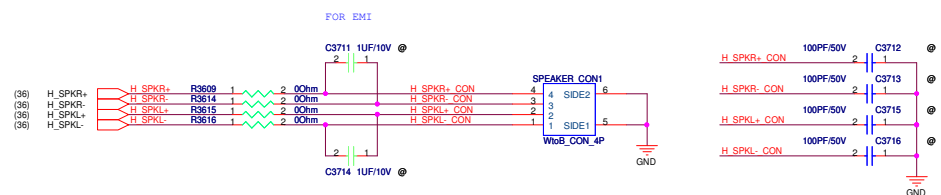


ANALOG MOAT

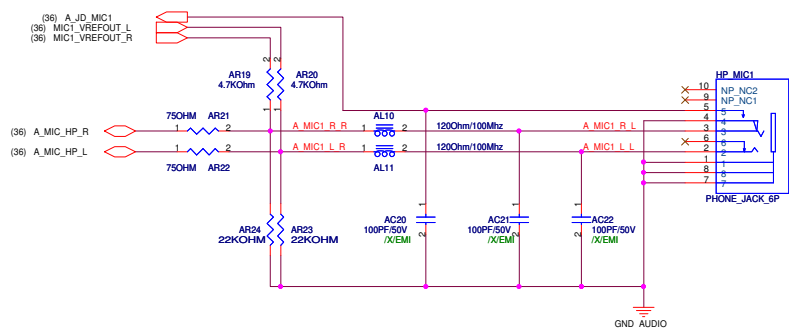
Update 11.08 (R2.0)



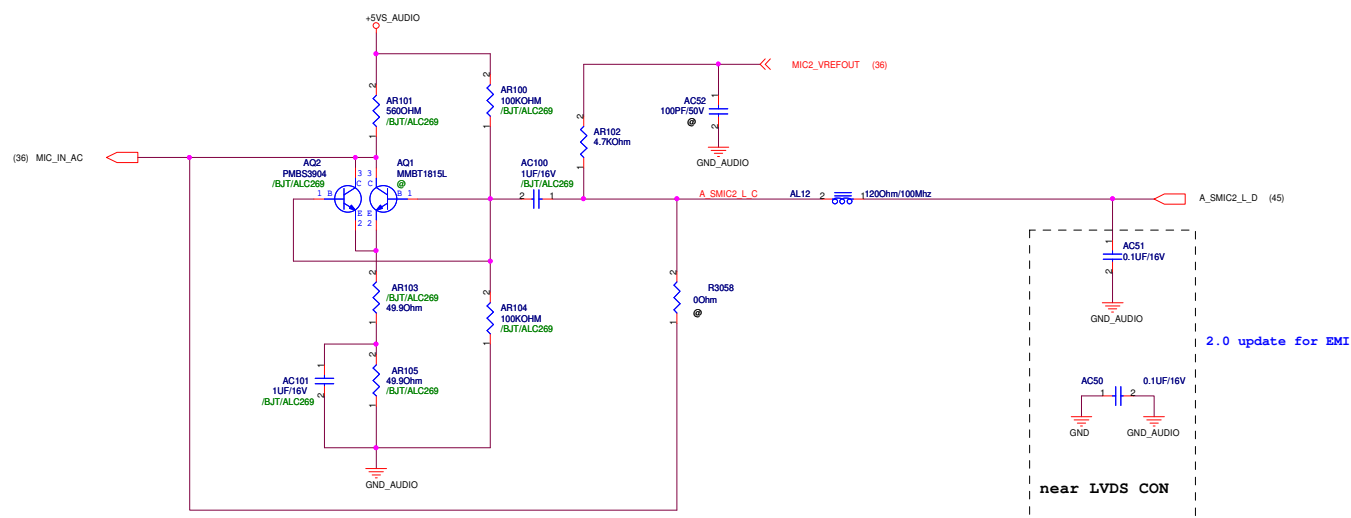
HP and MIC

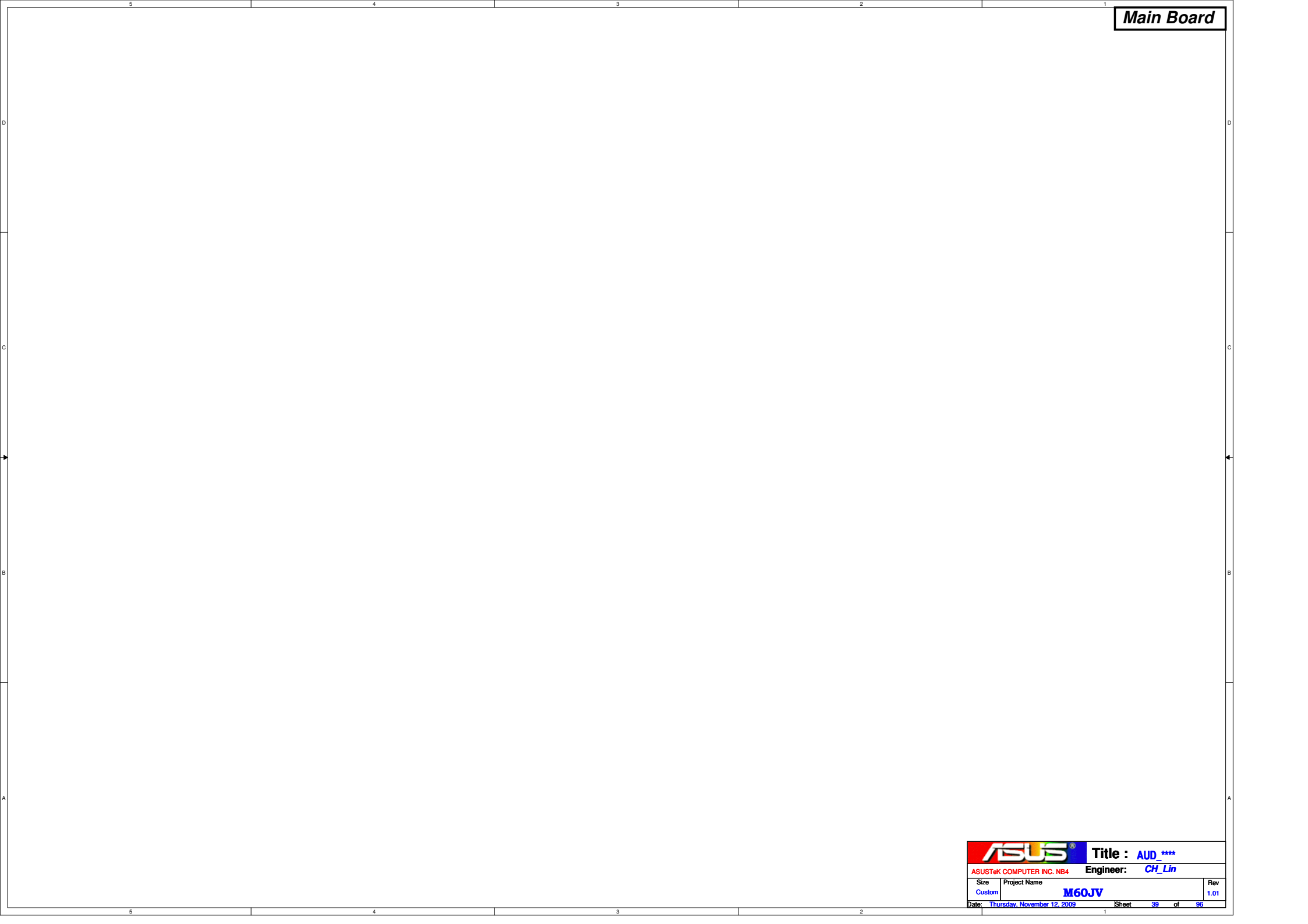


HP and MIC



Internal MIC and AMP








Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.

<Variant Name>

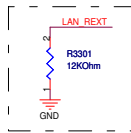
**Title :** AU6433D53-GLF

Engineer: Fehling_Wang

Size	Project Name	Rev
A3	1008P Card Reader	1.0G

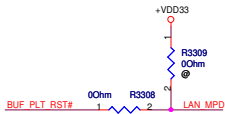
Date: Thursday, November 12, 2009Sheet 40 of 96

Reference Resistance

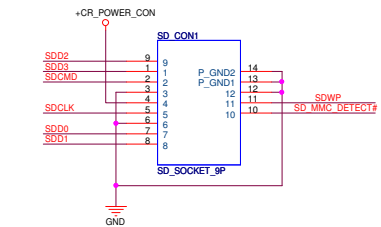
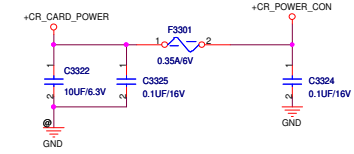
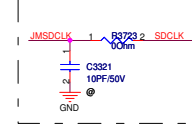
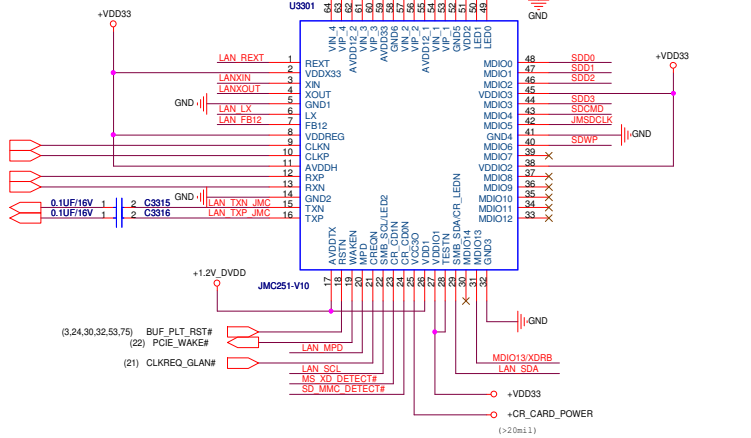


D3E Enable/Disable

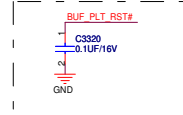
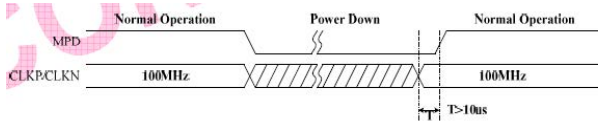
R3309	R3308	D3E
Unmount	Mount	Enable
Mount	Unmount	Disable



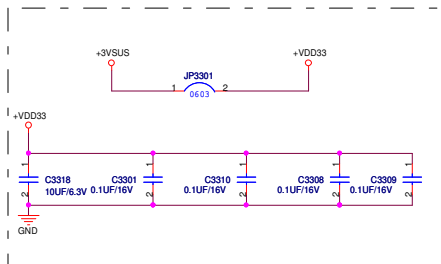
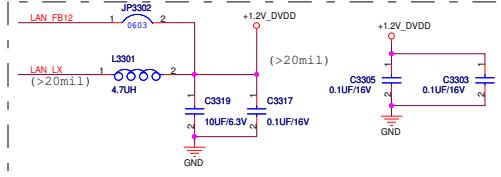
- (21) PCH_C_LAN_N
- (21) PCH_C_LAN_P
- (21) POE_TX_LAN_P
- (21) POE_TX_LAN_N
- (21) POE_RX_LAN_N
- (21) POE_RX_LAN_P



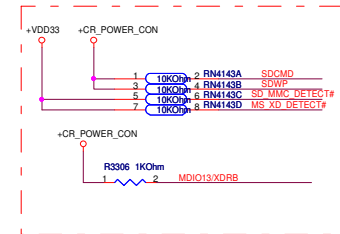
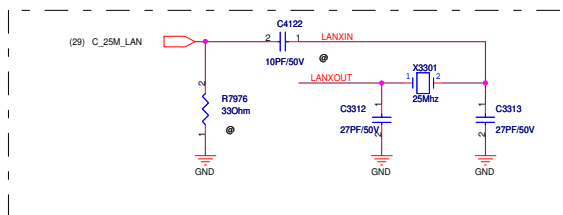
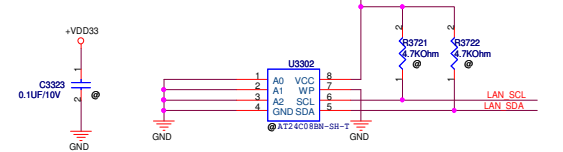
Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.




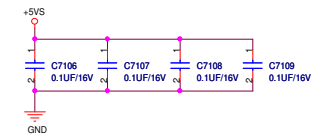
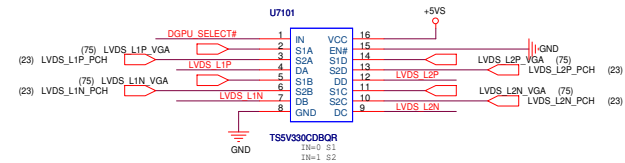
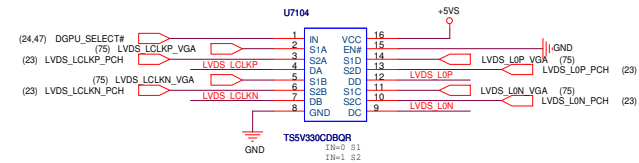
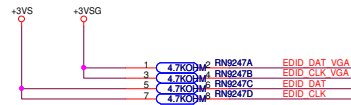
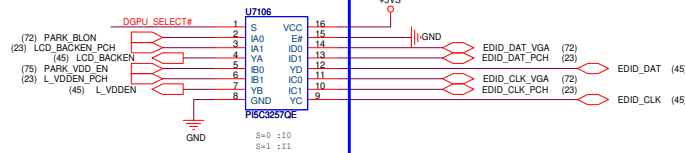
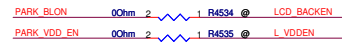
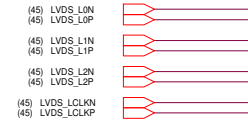
Switch Regulator



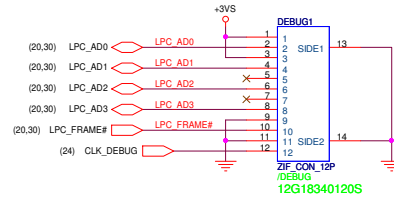
Serial EEPROM

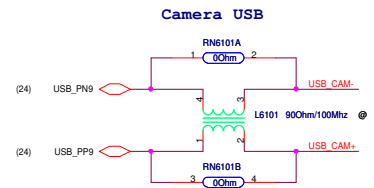
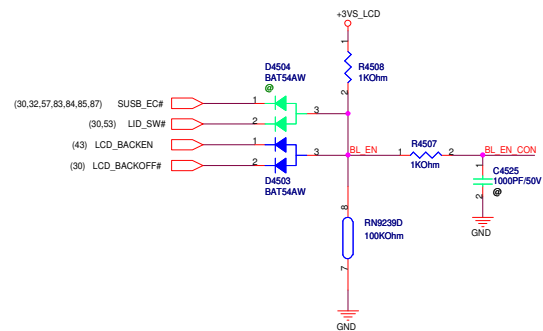
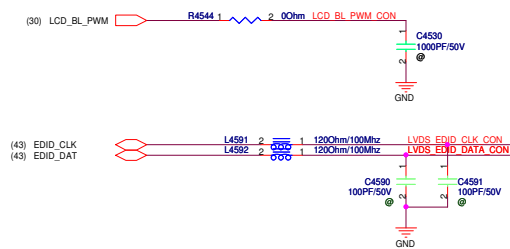
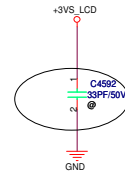
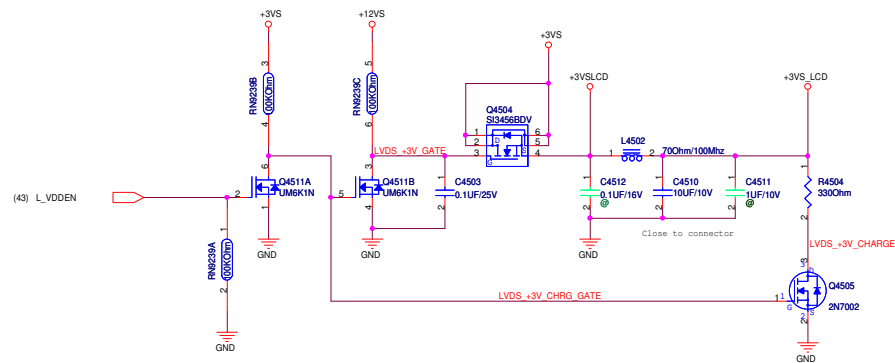


		Title : LAN_RJ45	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size Custom	Project Name M52J		Rev 1.3
Date: Thursday, November 12, 2009		Sheet 42	of 99

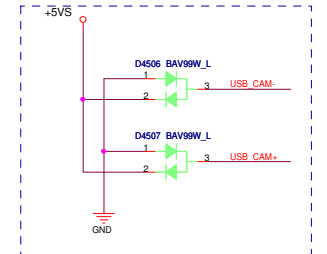


LPC Debug Port

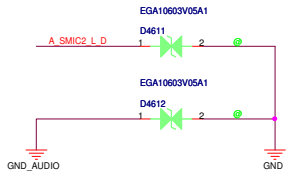
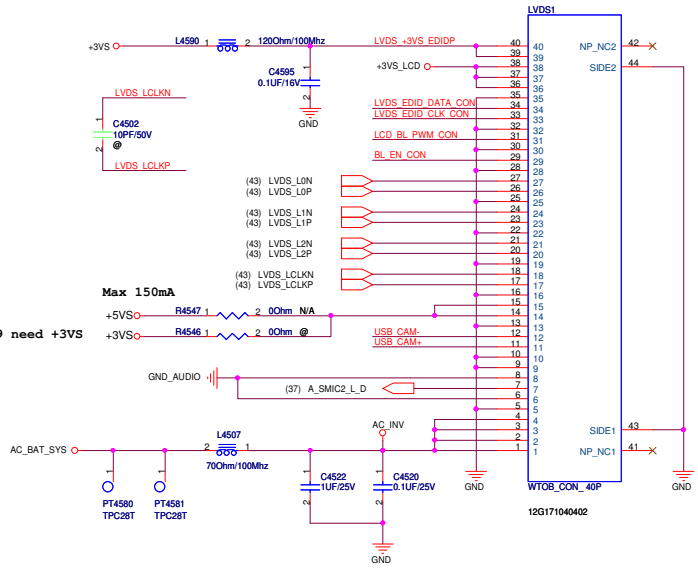


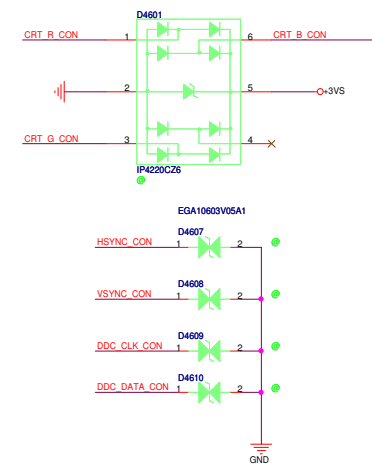
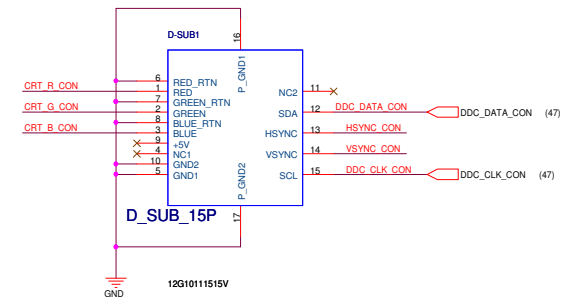
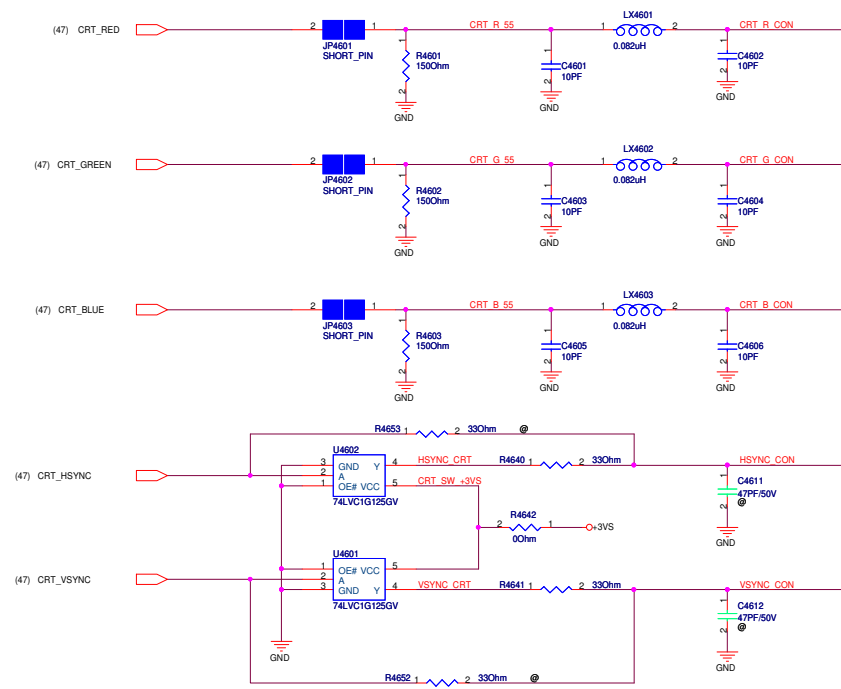


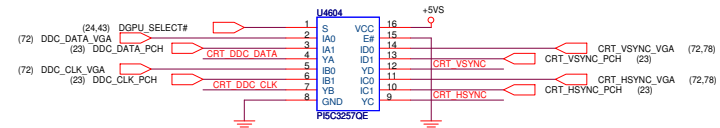
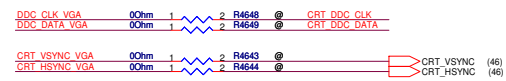
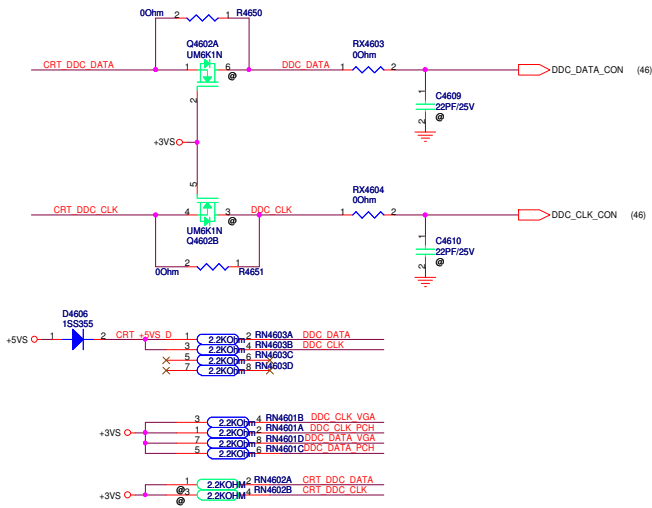
1.0 EMI test need mount D4506 and D4507



CNF9059 need +3VS

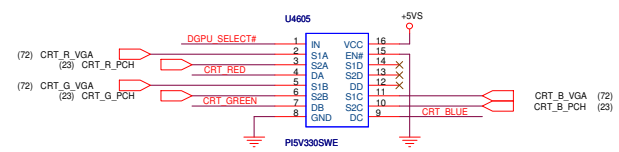






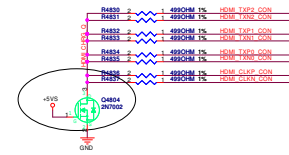
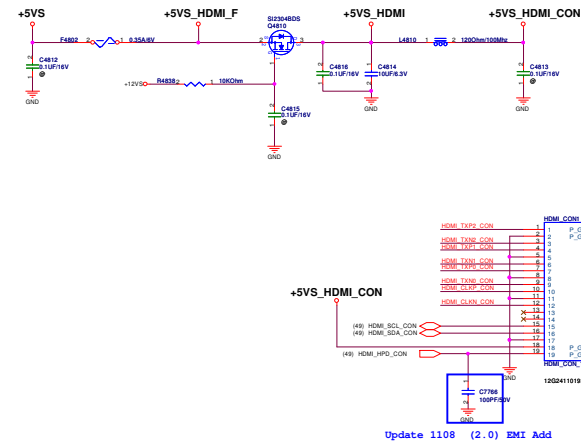
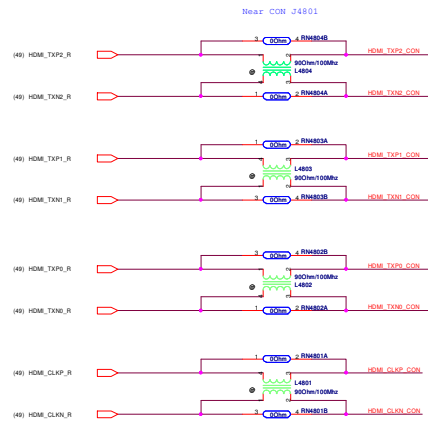
change pin define
A0 TO A1

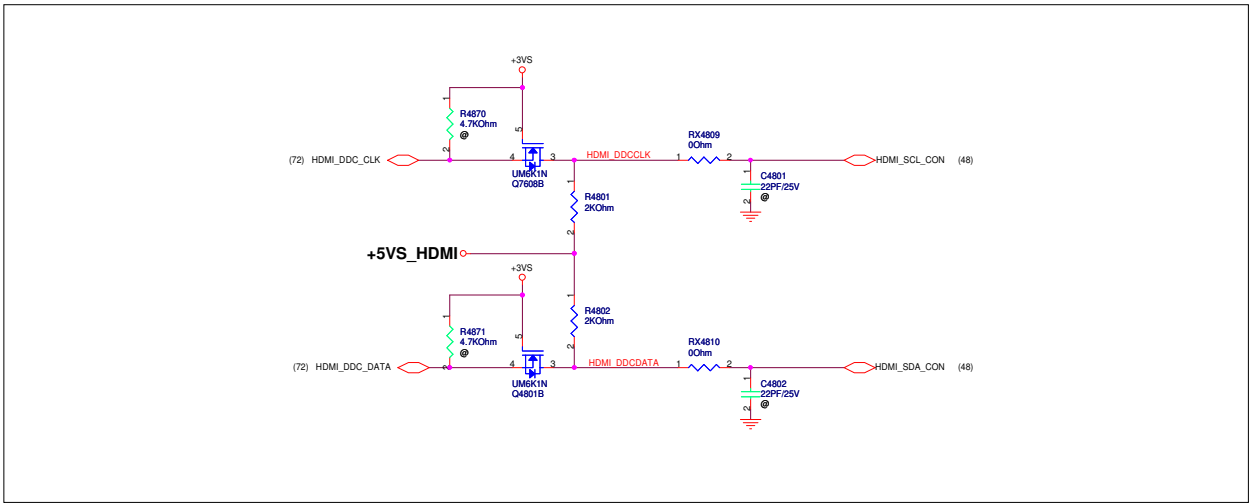
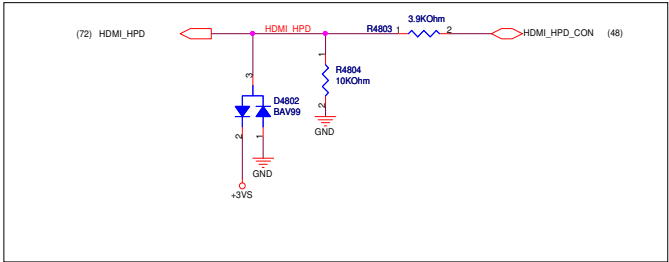
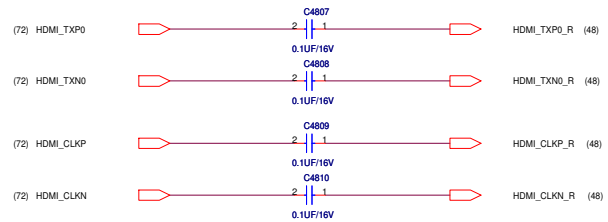
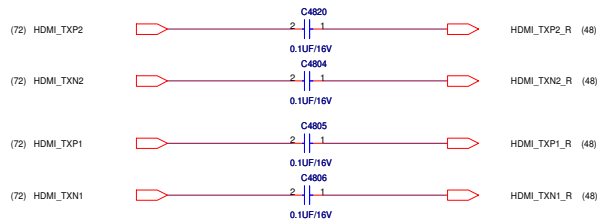
S=0 for VGA output
S=1 for PCH output



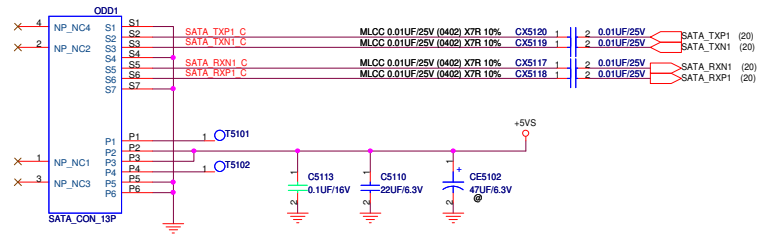
PI5V330SWE bandwidth=570MHz
PCH analog RAMDAC=350MHz.
(2048x1536 with 32bit color at 75Hz)

S=0 for VGA output
S=1 for PCH output

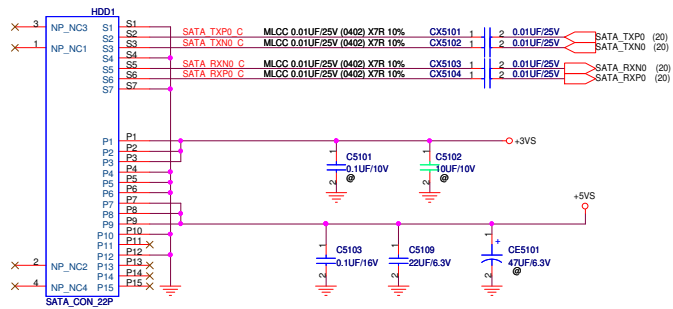




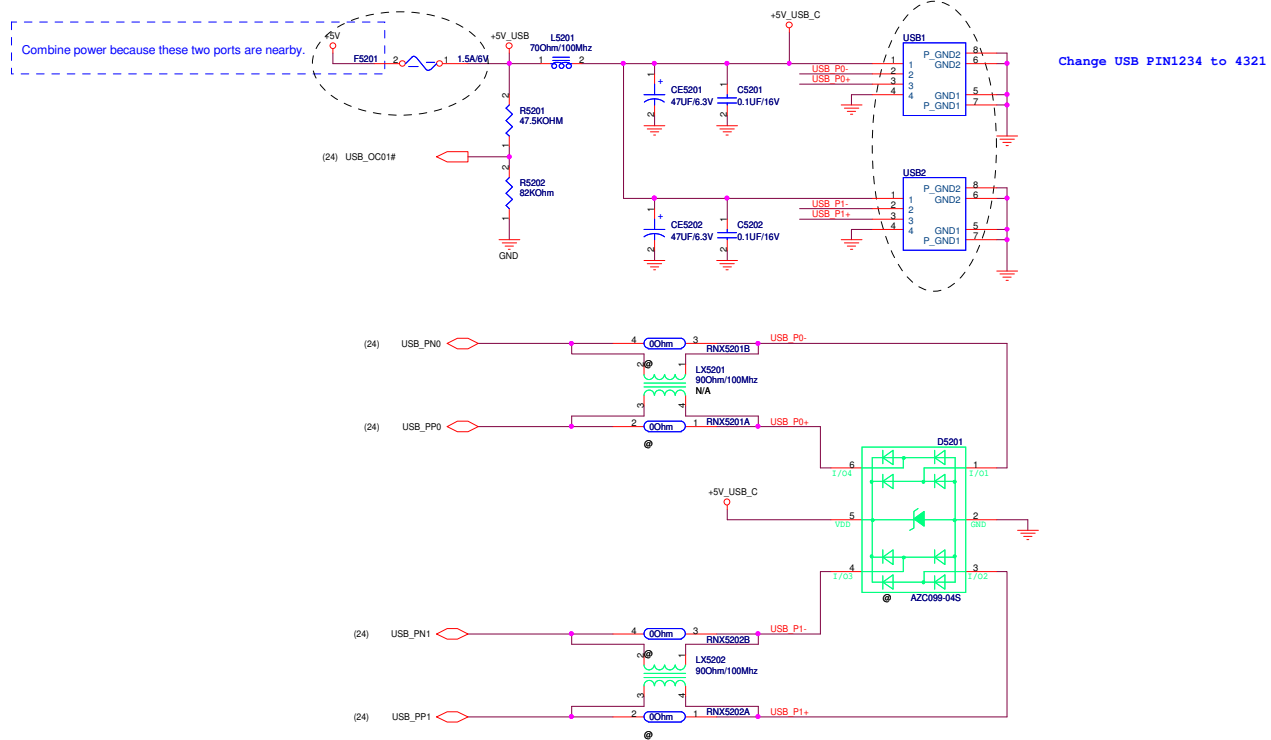
ODD

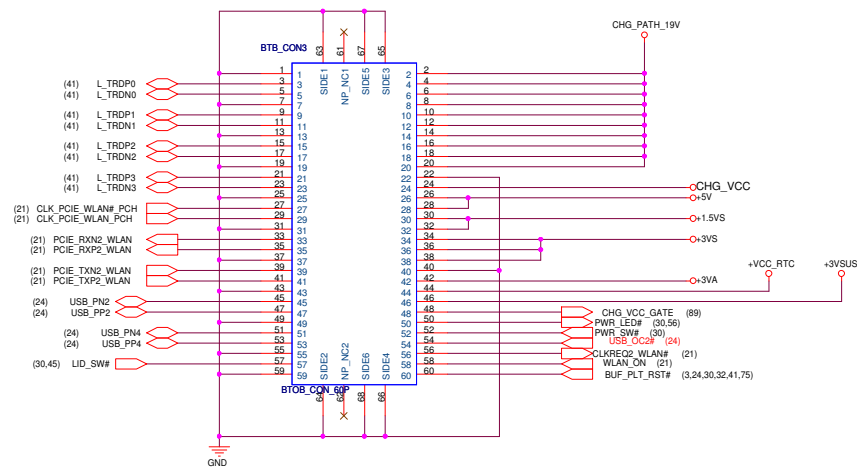


HDD (1st)

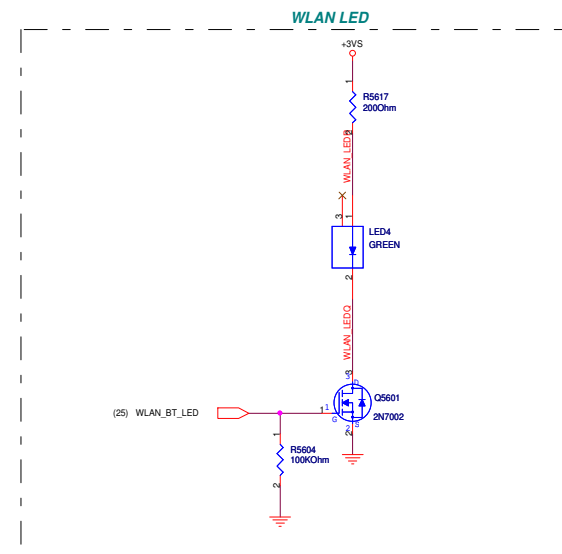
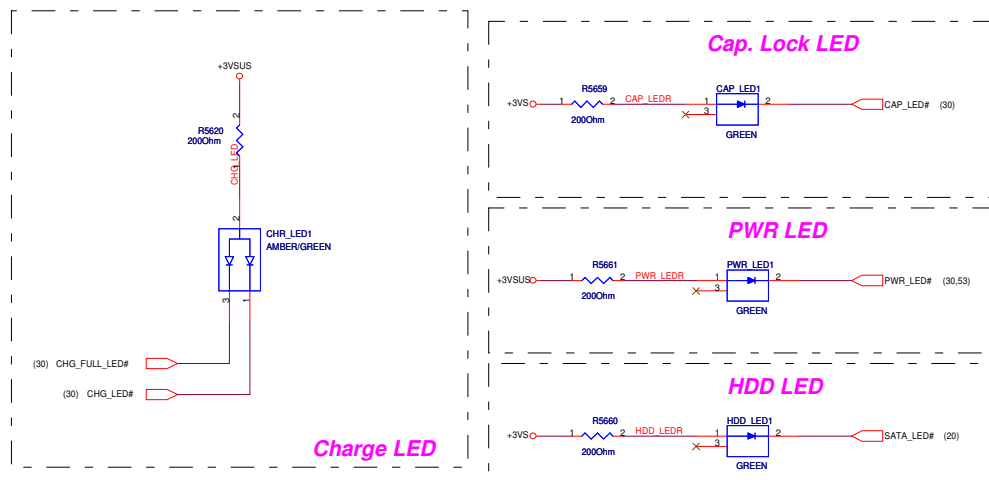


USB ports

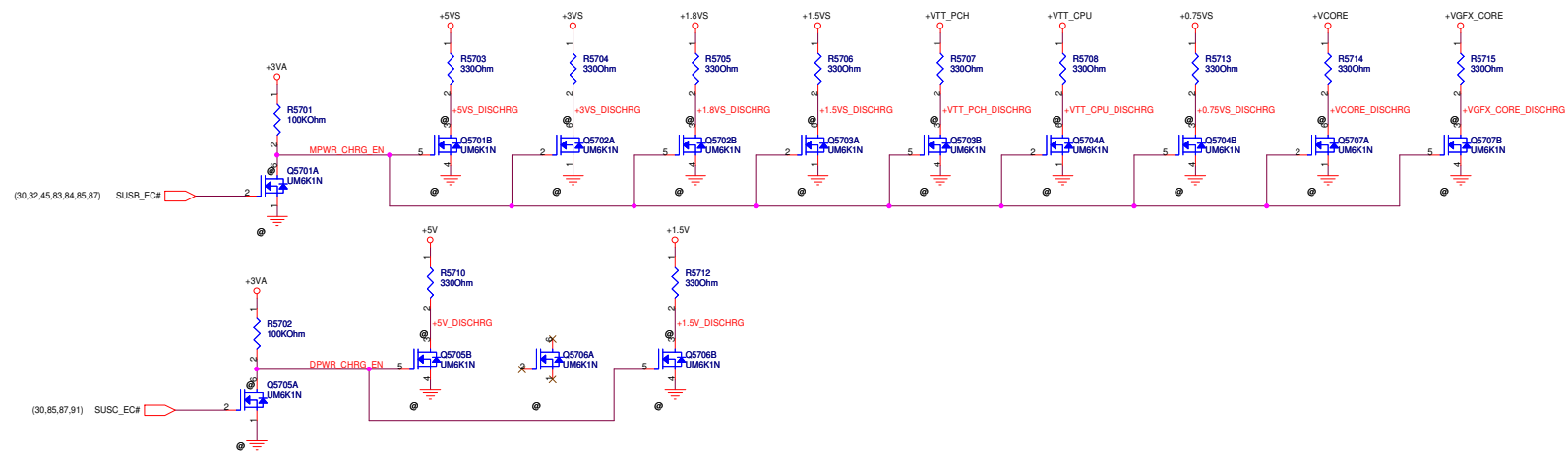





Main Board



Change LED part number



Main Board



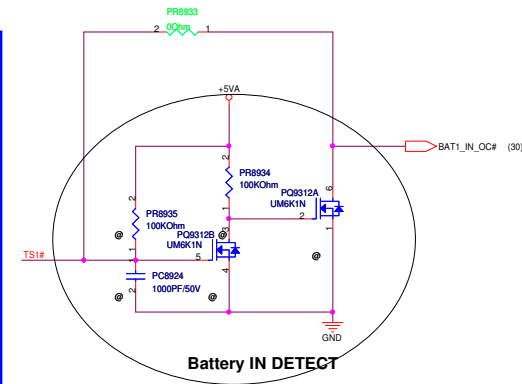
Title : DJ ****

ASUSTeK COMPUTER INC. NBD

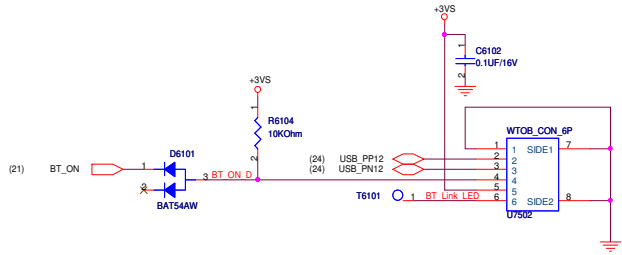
Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

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[illegible]

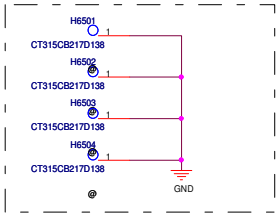
BLUETOOTH



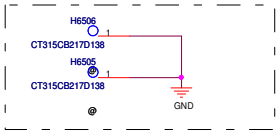


Main Board

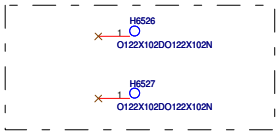
For CPU



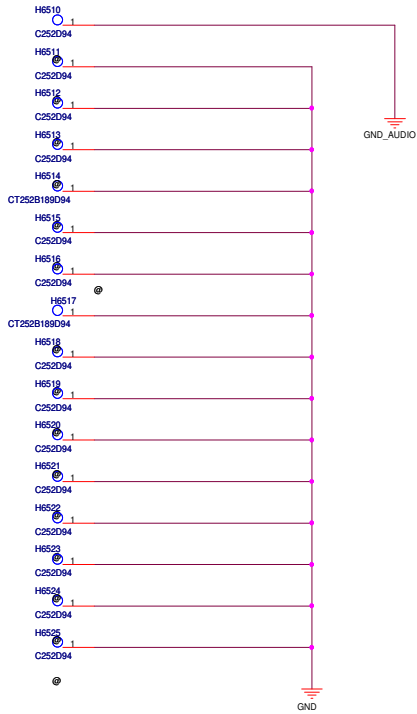
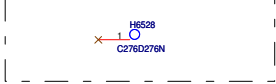
For GPU

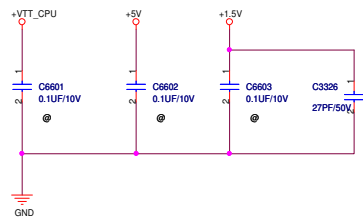


For 橢圓定位孔



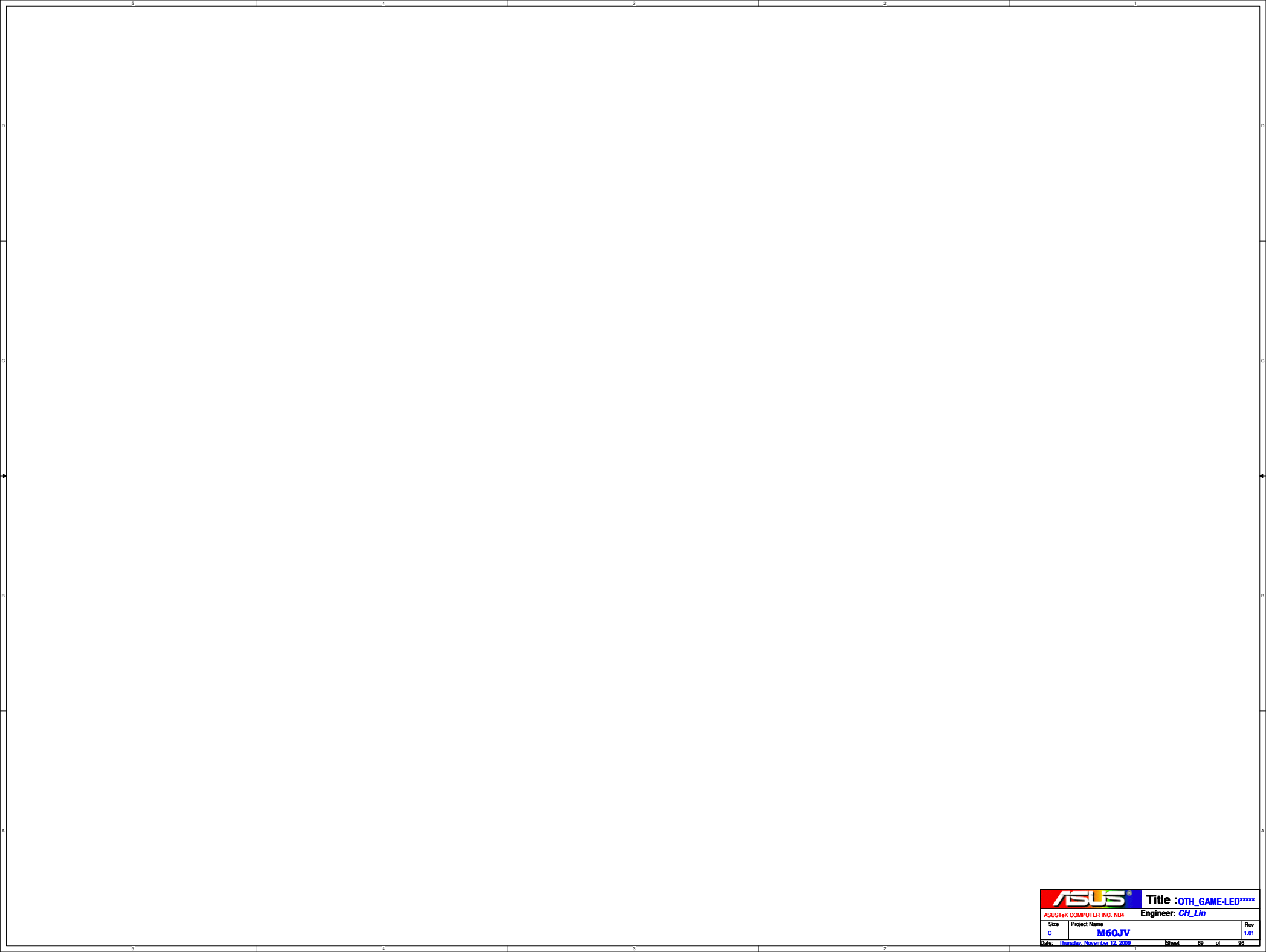
HHD 呼吸孔







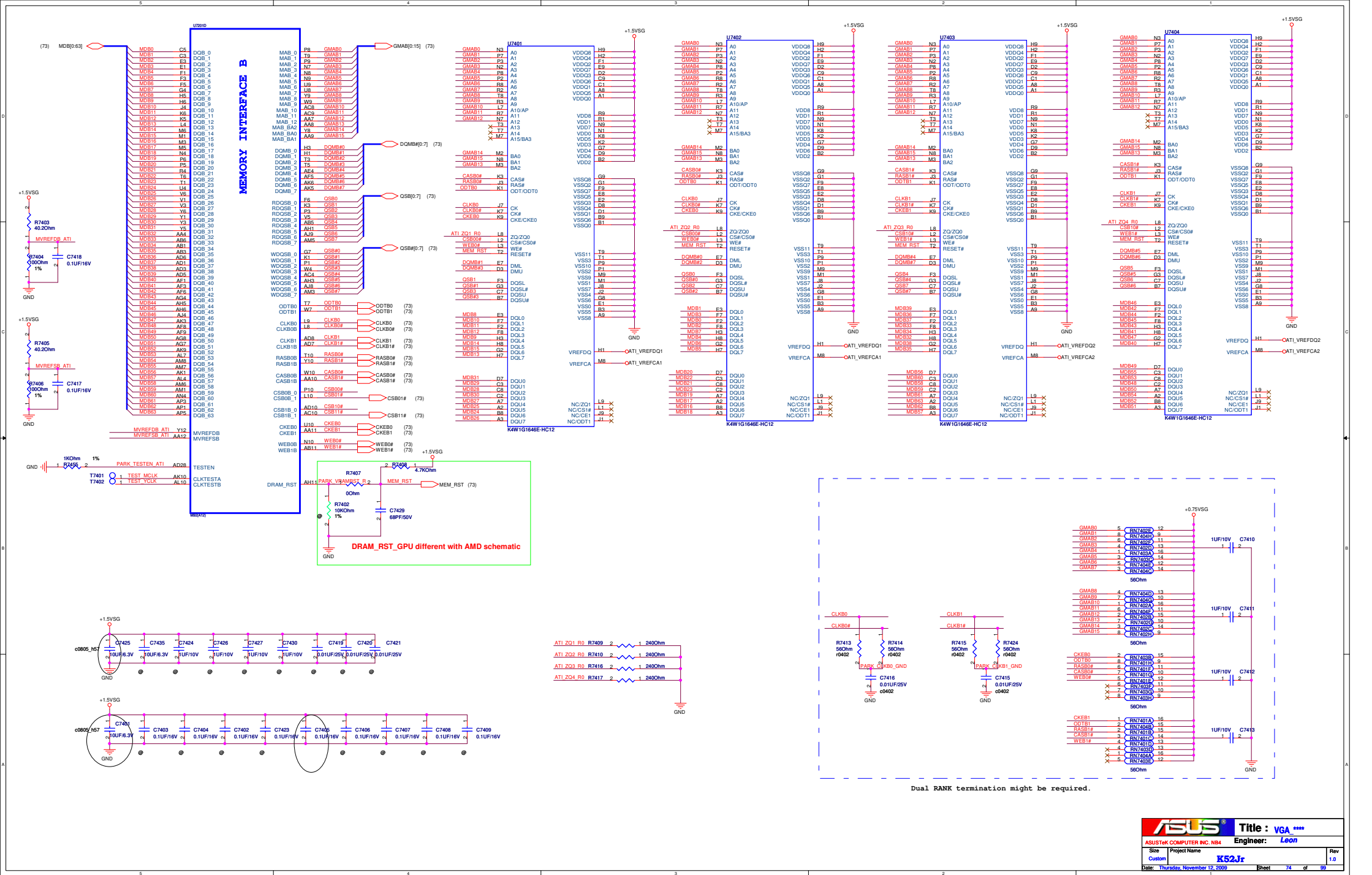






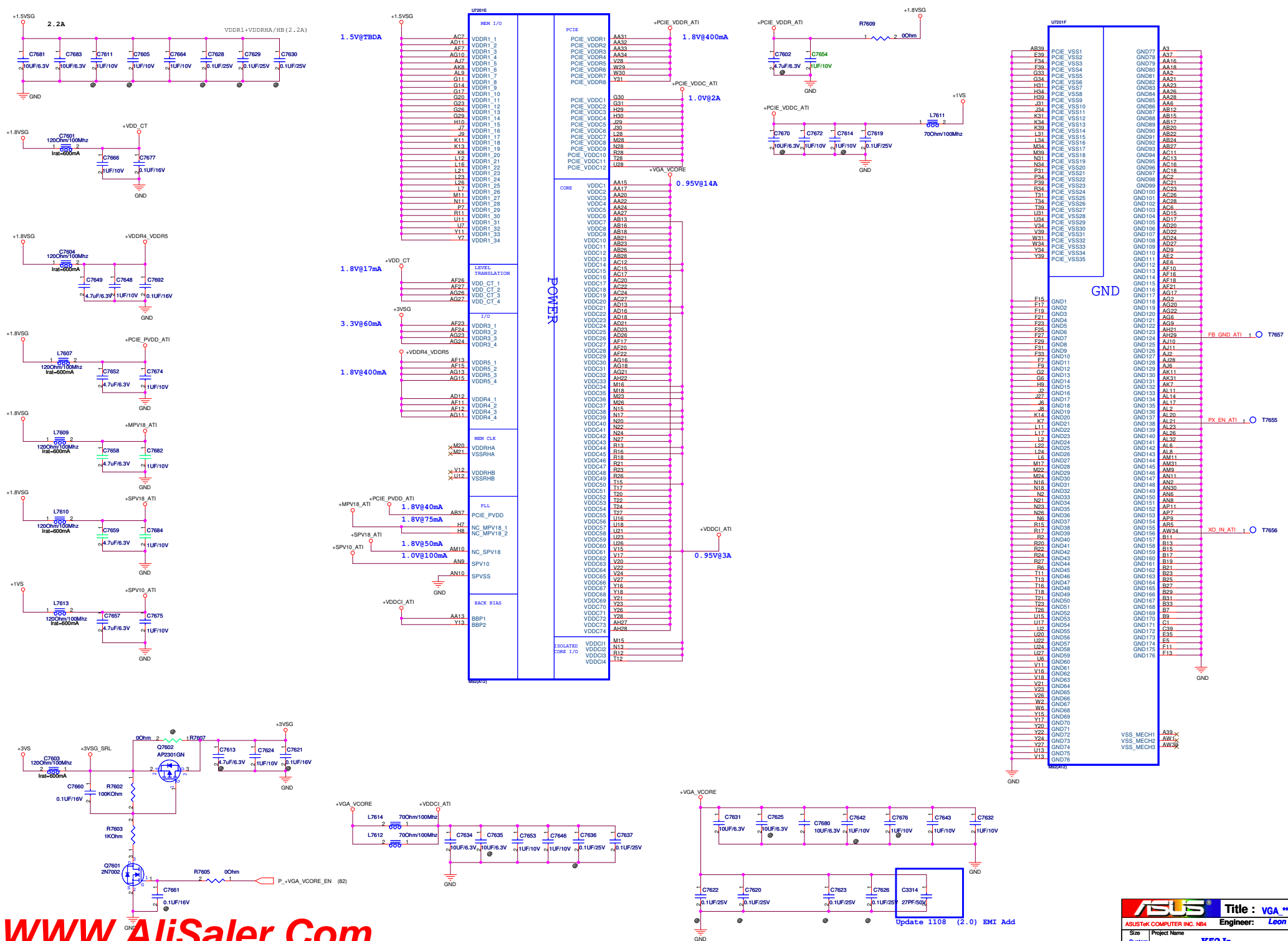
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Size Custom	Project Name M60JV		Rev 1.01
Date: Thursday, November 12, 2009		Sheet	70 of 96



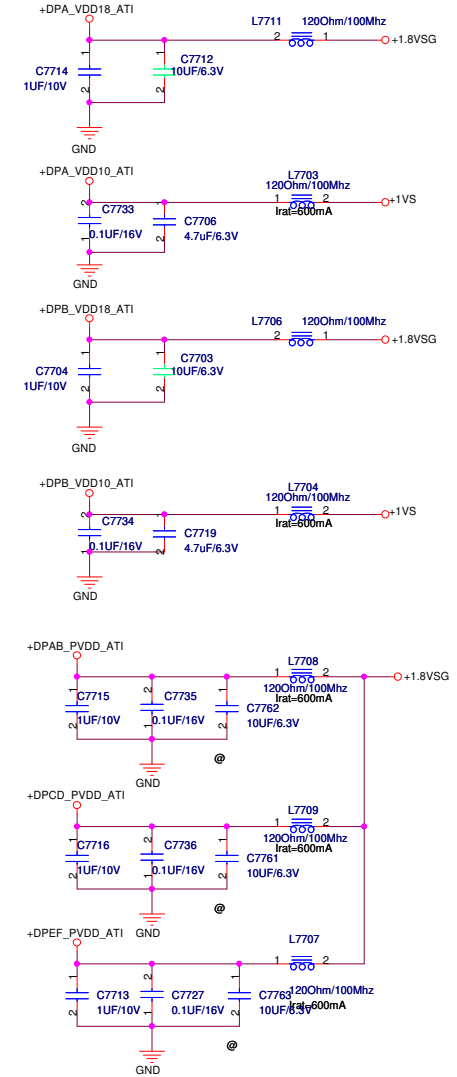
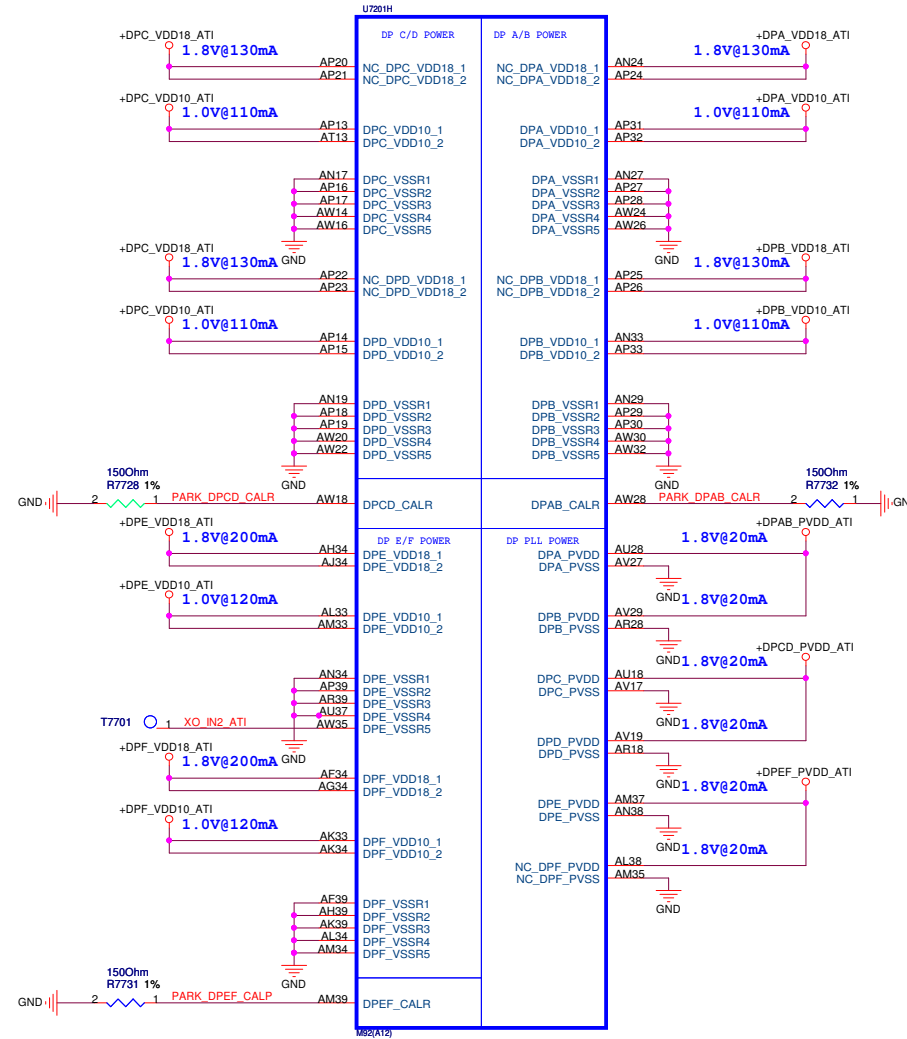
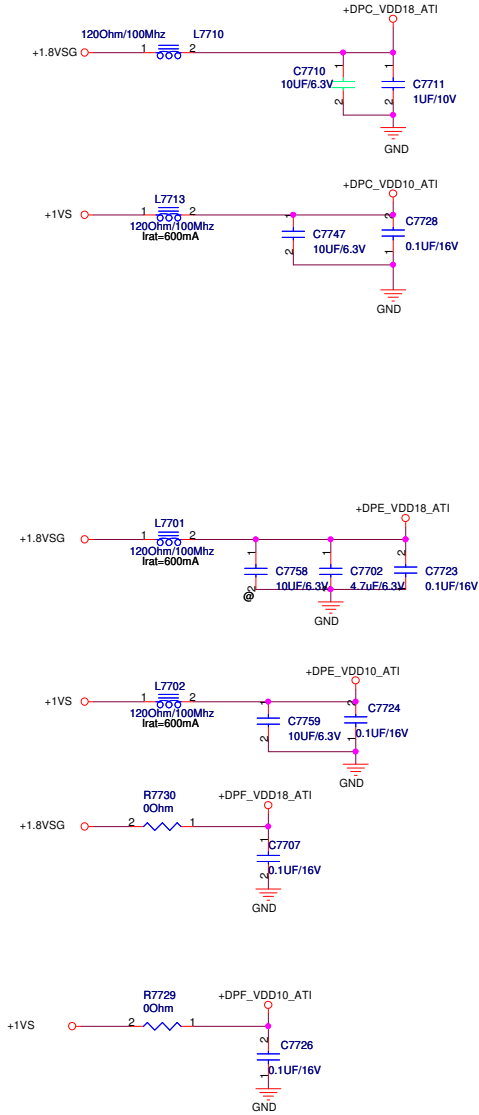


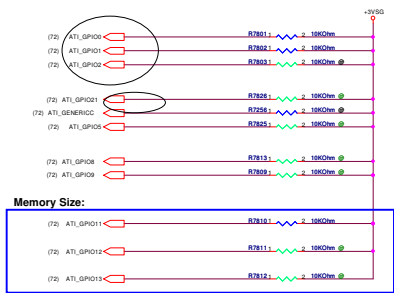
U7201A



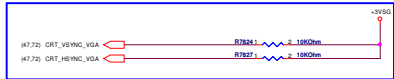


DPE: LVDS
DPB: HDMI
DAC1: CRT

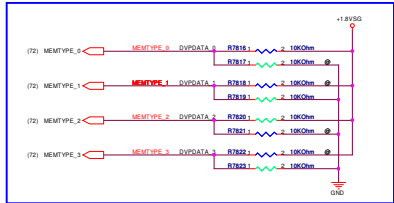




Audio function:



Memory Type:



Dual Rank DDR3 1GB need AMD check pull low or high for following DDR3 VRAM			
03G151638020	DDR3	64M*16-1.2 FBGA-96	SAMSUNG/K4W1G1646E-HC12
03G151638421	DDR3	64M*16-1.2 FBGA-96	HYNIX/H5TQ1G63BFR-12C

Vendor	DVPG47A2.1.2 ID	ID	DDR Memory Type	Channel Size
Infineon (Qimonda)	0000	0	320M x32 (2GB)	A channel(M0-M2); 8 channel(M0-M7)
	0001	1	320M x32 (2GB)	2-AB channel
	0002	2	320M x32 (2GB)	A channel(M0-M2); 8 channel(M0-M7)
	0003	3	640M x32 (4GB)	2-AB channel
Samsung	0010	0	640M x32 (4GB)	A channel(M0-M2); 8 channel(M0-M7)
	0011	1	320M x32 (2GB)	2-AB channel
	0012	2	320M x32 (2GB)	A channel(M0-M2); 8 channel(M0-M7)
	0013	3	640M x32 (4GB)	2-AB channel
Hynix	1000	0	320M x32 (2GB)	A channel(M0-M2); 8 channel(M0-M7)
	1001	1	320M x32 (2GB)	2-AB channel
	1002	2	640M x32 (4GB)	A channel(M0-M2); 8 channel(M0-M7)
	1003	3	640M x32 (4GB)	2-AB channel
Elpida	1100	0	320M x32 (2GB)	A channel(M0-M2); 8 channel(M0-M7)
	1101	1	320M x32 (2GB)	2-AB channel
	1102	2	640M x32 (4GB)	A channel(M0-M2); 8 channel(M0-M7)
	1103	3	TBD	TBD

Vendor	DVIDATA3.2.3.1	ID	DDR Memory Type	Channel Size
Gimonda	0000	0	32GB (2 x 16GB)	B channel
	0001	1	32GB (2 x 16GB)	B channel
	0002	2	32GB (2 x 16GB)	B channel
Samsung	0011	0	4GB (2 x 2GB)	B channel
	0012	1	4GB (2 x 2GB)	B channel
	0110	6	4GB (2 x 2GB)	B channel
Hynix	0111	0	32GB (2 x 16GB)	B channel
	0112	1	32GB (2 x 16GB)	B channel
	0113	10	4GB (2 x 2GB)	B channel
	1100	12	4GB (2 x 2GB)	B channel
	1101	13	TBD	B channel
	1110	14		B channel

M92-M2 only support 8 channel

TX_PWRS_ENB	GPIO_0	<p>Transmitter Power Savings Enable</p> <p>0: 50% Tx output swing. Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the P.O.I Express – Mobile Graphics Low-Power Addendum).</p> <p>1: Full Tx output swing.</p>	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements) Otherwise: Must be pulled to 3.3 V at reset using ~3-K (5%) resistor
TX_DEEMPH_EN	GPIO_1	<p>PCI Express Transmitter De-emphasis Enable</p> <p>0: Tx de-emphasis disabled. Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the P.O.I Express – Mobile Graphics Low-Power Addendum).</p> <p>1: Tx de-emphasis enabled.</p>	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements) e.g. motherboard implementations.) Otherwise: Must be pulled to 3.3 V at reset using ~3-K (5%) resistor (e.g. MCM and add-in boards).
BIF_0EN2_EN_A	GPIO_2	<p>0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.</p> <p>Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CBB (compliance base board).</p>	0 (Internal pull-down)	0 5.0 GT/s capability will be controlled by software.
VGA_DIS	GPIO_8_ROMSI	<p>VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).</p> <p>0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller.</p>	0 (Internal pull-down)	0 Do not populate. Provide pad with output to pull to 3 V (VDDR3).
CONF10[2] CONF10[1] CONF10[0]	GPIO_12 GPIO_13 GPIO_11	<p>If BIOS_ROM_EN = 1, then CONF12[2] defines the ROM type. See "RCM Configuration" on page 3-33</p> <p>If BIOS_ROM_EN = 0, then CONF12[2] defines the primary memory aperture size. See "Primary Memory Aperture size requested at PCI Configuration" on page 3-33</p>	0 (Internal pull-down)	Design dependent. See description for more information.

BIOS_ROM_EN	GPIO_Z22_ROMCSB	<p>Enable external BIOS ROM device</p> <ul style="list-style-type: none"> 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device 	0 (internal pull-down)	Design dependent. See description for more information.
AUD[1] AUD[0]	HVSNC VSVNC	<p>AUD[1]:0 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.</p> <p>HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.</p>	0 (internal pull-down)	Design dependent. See description for more information.
VIP_DEVICE_STRAP_EN	V28VNC	<p>VIP Device Strap Enable indicates to the software driver that it should try to sense whether or not a VIP device is connected on the VIP Host interface.</p> <ul style="list-style-type: none"> 0 - Driver would ignore the value sampled on VH4D_0 during reset 1 - Driver would use the value sampled at reset from VH4D_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no). According to the VIP 1.1 standard, VH4D_0 is tied high, and VIP slave devices are required to drive this signal low during reset. This scheme allows for a VIP device to be connected to the graphics adapter via a daughter card. <p>Note: If the strap is needed, it must be placed between the ball and the VSVNC output buffer. This output buffer prevents monitors from affecting the value at reset.</p>	0 (internal pull-down)	Design dependent. See description for more information.

RESERVED CONFIGURATION STRAPS

Allow for pull-up pads for these straps and if these GPIOs are used, they must not conflict during reset

RESERVED	H2B5YNC	Internal use only. This PAD has an INTERNAL PULL-DOWN and MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except 0ND at reset.	0	Internal pull-down	Do not populate. Provide a pull-up resistor to pull to 1 V (VDDR3).
Push up pads are not required for these straps but if these straps are used, they must not conflict during reset.					
RESERVED	GPI0_2_ROMIO GPIO_21_B0_EN	Internal use only. These PADS HAVE INTERNAL PULL-DOWNS and MUST BE 0 V AT RESET. These pads may be left unconnected, however, if they are connected to additional logic on the board, the logic must not allow these signals to be driven or pulled to any value except 0ND at reset.	0	Internal pull-down	No PAD required. Ensure that no logic conflicts with these signals during Reset.

Pull-up pads are not required for these straps but if these GPIOs are used, they must not conflict during reset.

RESERVED	GPIO_0_ROMIO GPIO_X1_BIF_EN	Internal use only. THESE PADS HAVE INTERNAL PULL-DOWNS AND MUST BE 0 V AT RESET. These pads may be left unconnected, however, if they are connected to additional logic on the board, the logic must not allow these signals to be driven or pulled to any value except GND at reset.	0 (internal pull-down)	No PAD required. Ensure that no logic conflicts with these signals during Reset.
64 MB		010		
32 MB		011		
512 MB		Not Supported		
1 GB		Not Supported		
2 GB		Not Supported		
4 GB		Not Supported		


POWERPLAY Interface

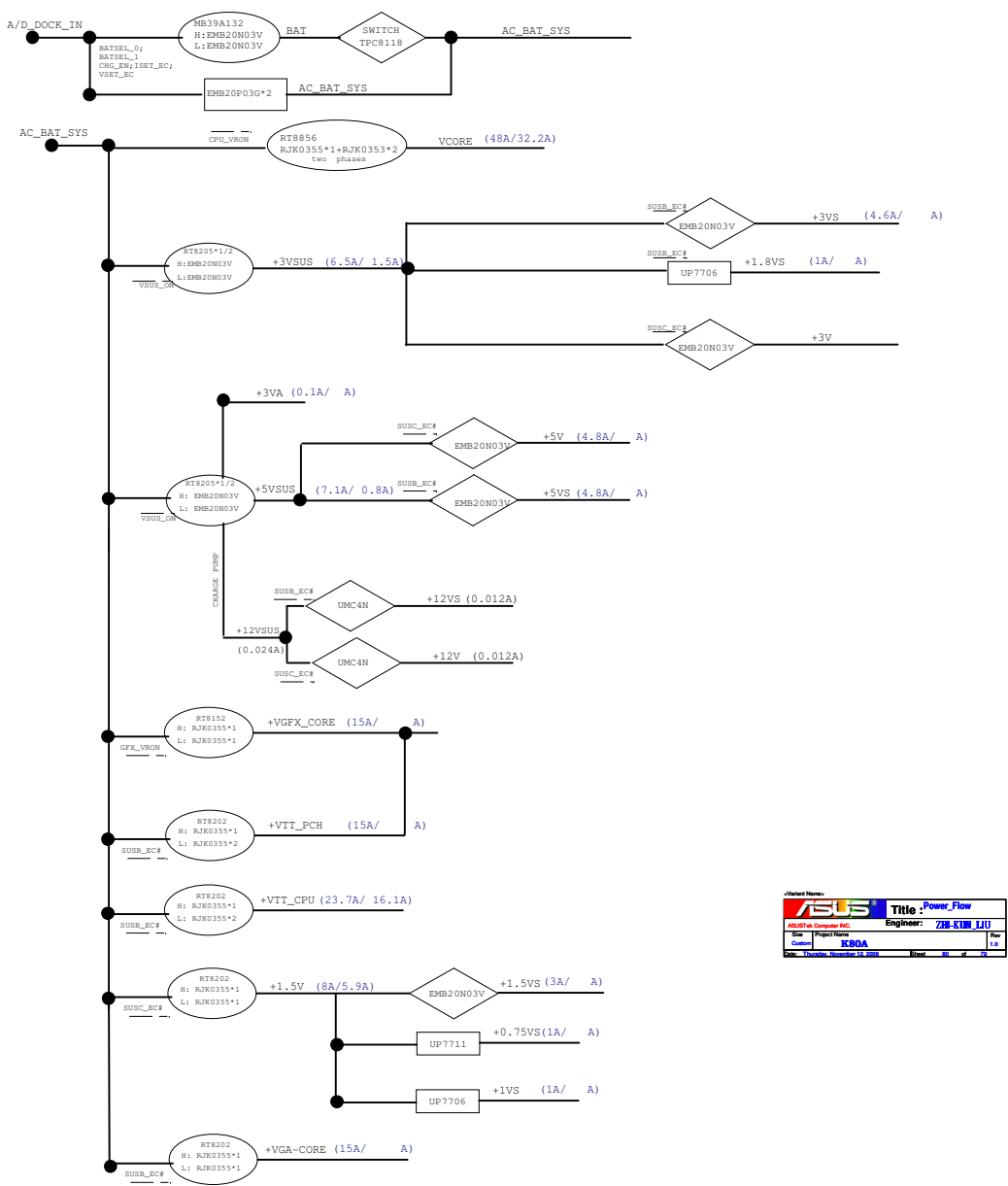
Pin Name	Type	PdPU	Description
GPIO_5_A0_BATT	I/O	PD-reset	GPIO_5_A0_BATT is an optional input which allows the system to request a fast power reduction by setting GPIO_5_A0_BATT to low (0V). The resulting state transition may disturb the display momentarily.
			Power reductions that are less than critical use the standard software methods only in order to prevent display disturbances.
GPIO_6	I/O	PD-reset	Voltage control signals for the core (VDDC and VDDCI).
GPIO_16_PWRCTRL_0	I/O	3.3V	At Reset, these signals will be inputs with weak internal pull-up resistors.
GPIO_16_PWRCTRL_1	I/O	3.3V	GPIOs can define all voltage control signals to be either 3.3V or open drain outputs (all signals must be the same type).
			The output state (high/low) of these signals is programmable for each PowerPlay state.
GPIO_16_BB_EN	I/O		Optional Voltage control for memory voltage regulator. Note that this signal must be low (0 V) at Reset (failure to do so will prevent boot).

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				RECOMMANDED SETTINGS R = DO NOT RESET RESISTOR P = INTERNAL 10K RESISTOR A = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		
TX_PWRN_ENB	GPI00	PCI0 FULL TX OUTPUT SWING		X
TX_DEEMPH_EN	GPI01	PCI0 TRANSMITTER DE EMPHASIS ENABLED		X
RESERVED	GPI04	RESERVED		0
REF_VIOA[0:5]	GPI08	VIOA FINALEO		0
RESERVED	GPI09	RESERVED		0
BIOS_ROM_EN	GPI0_22_IOMC08	ENABLE EXTERNAL BIOS ROM		X
ROMDCFG[0:2]	GPI0[3:11]	SERIAL ROM / OR MEMORY APERTURE SIZE SELECT		X X X
VIP_DEVICE_STRAP_ENA	V25VNC	IGNORE VIP DEVICE STRAPS		X
RSVD	HS2VNC			0
RSVD	GENERIC0			0
AUD[0]	HS2VNC	SEE DATABOOK FOR DETAIL		X
AUD[8]	V19VNC	SEE DATABOOK FOR DETAIL		X

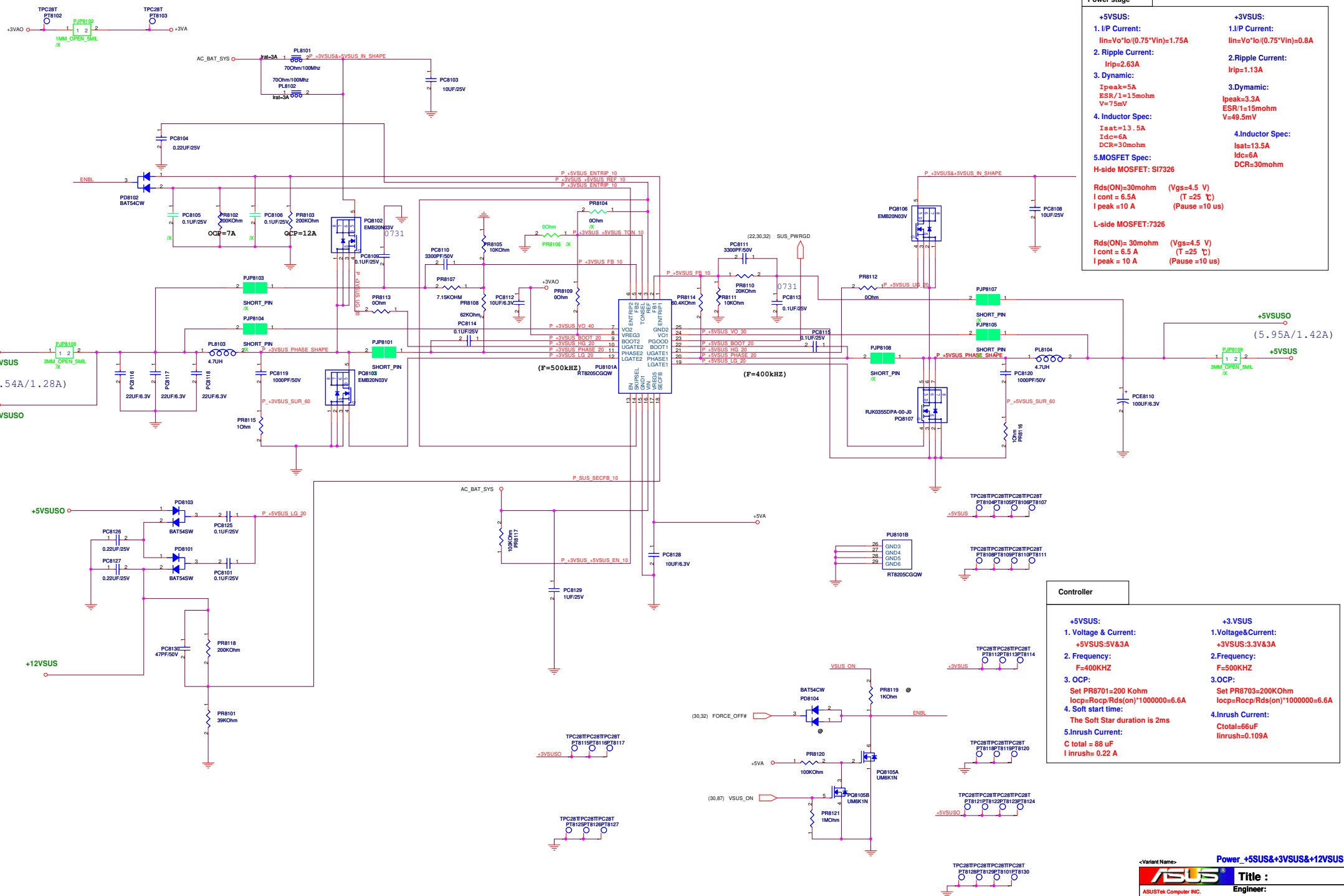
AMD RESERVED CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
HS2VNC	GENERIC0	GPI02	GPI021	



		Title : VGA_M96_STRAP	
ASUSTeK COMPUTER INC. NB4		Engineer: Leon	
Size A3	Project Name K52Jr		Rev 1.0
Date: Thursday, November 12, 2009		Sheet	79 of 99



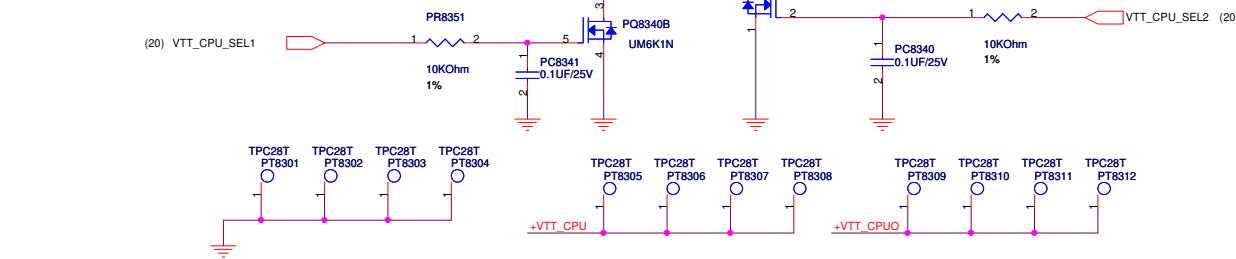
ASUS		Title: Power Flow	
ASUS AIoT & Computer PC		Engineer: ZHAO KUN LIU	
Date	Project Name	Rev	1.0
Checked	KRQA		
Date: 2023-08-10 14:00:00			



Power stage	
+5VSUS: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.75A$ 2. Ripple Current: $I_{peak} = 5A$ $ESR / 1 = 1.5mohm$ $V = 75mV$ 3. Dynamic: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 4. Inductor Spec: $R_{ds(ON)} = 30mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 10A$ (Pause = 10 us)	+3VSUS: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.8A$ 2. Ripple Current: $I_{rip} = 1.13A$ 3. Dynamic: $I_{peak} = 3.3A$ $ESR / 1 = 15mohm$ $V = 49.5mV$ 4. Inductor Spec: $R_{ds(ON)} = 30mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 10A$ (Pause = 10 us)
5. MOSFET Spec: H-side MOSFET: SI7326 L-side MOSFET: 7326	

Controller	
+5VSUS: 1. Voltage & Current: +5VSUS: 5V & 3A 2. Frequency: $F = 400KHZ$ 3. OCP: Set PR8701 = 200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Soft start time: The Soft Star duration is 2ms 5. Inrush Current: $C_{total} = 88uF$ $I_{inrush} = 0.22A$	+3VSUS: 1. Voltage & Current: +3VSUS: 3.3V & 3A 2. Frequency: $F = 500KHZ$ 3. OCP: Set PR8703 = 200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Inrush Current: $C_{total} = 66uF$ $I_{inrush} = 0.109A$

VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%



Controller

- Voltage & Current:**
+VCCP:1.05V@10A
- Frequency:**
Ton=3.85p*Rt(on)/(Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ
- OCP:**
Set PR7343=18KOhm
Iocp=Rocp*20/Rds(on)=22A
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush Current:**
C total = 200 uF
I inrush= 0.16 A

Power stage

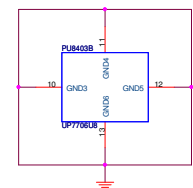
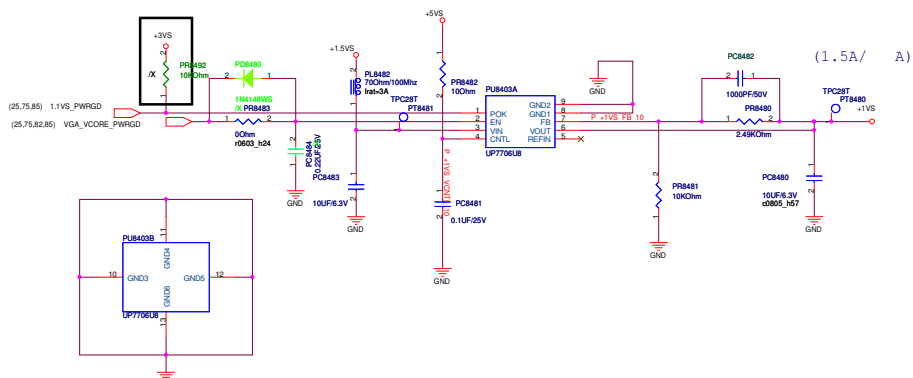
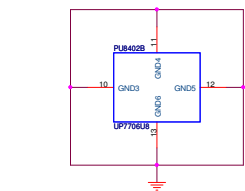
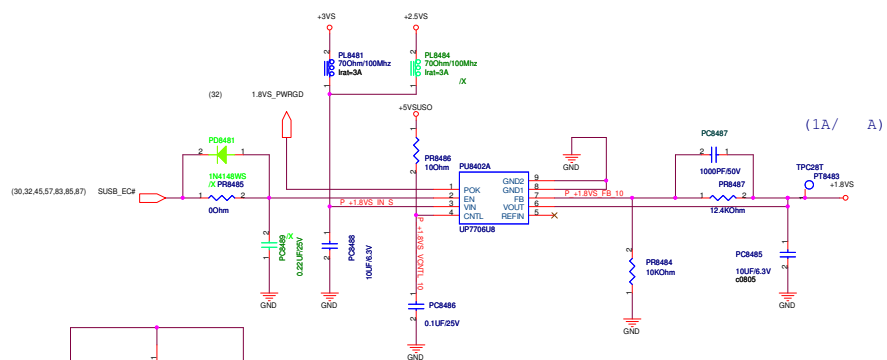
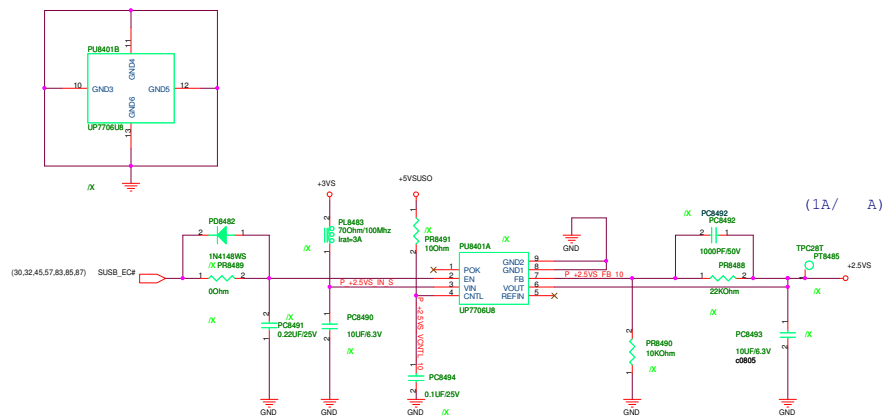
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.3 A$
- Ripple Current:**
Iripple=2.8A
- Dynamic:**
Ipeak=1.98A
DCR=3.3mohm
V=6.534mV
- Inductor Spec:**
Isat=16A
Idc=11A
DCR=9mOhm
- MOSFET Spec:**
H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

Title : Power_+VCCP

ASUSTeK COMPUTER INC
Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009
Sheet 83 of 1



Controller

1. Voltage & Current:

+1.8V; +1.8V & 12A

2. Frequency:

Ton=3.85p*Rt(on)*Vo/Vin-05
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:

Set PR7343=18kohm
Iocp=Rocp*20/Rds(on)
=20*1.5/16.5=26A

4. Soft start time:

Soft-Start duration is 1.35ms

5. Inrush Current:

C total =100uF

Inrush=0.133A

Power stage

1. IP Current:

I in = Vo/Io/(0.8 * Vin)=0.947A

2. Ripple Current:

Iripple=2.342A

3. Ripple Voltage:

Ipeak=(vin-v0)*D/(L*Fsw)=3.25A
DCR=3.3mohm
V=10.75mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mohm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTek COMPUTER INC

Size Project Name

Custom

Date: Thursday, November 18, 2009

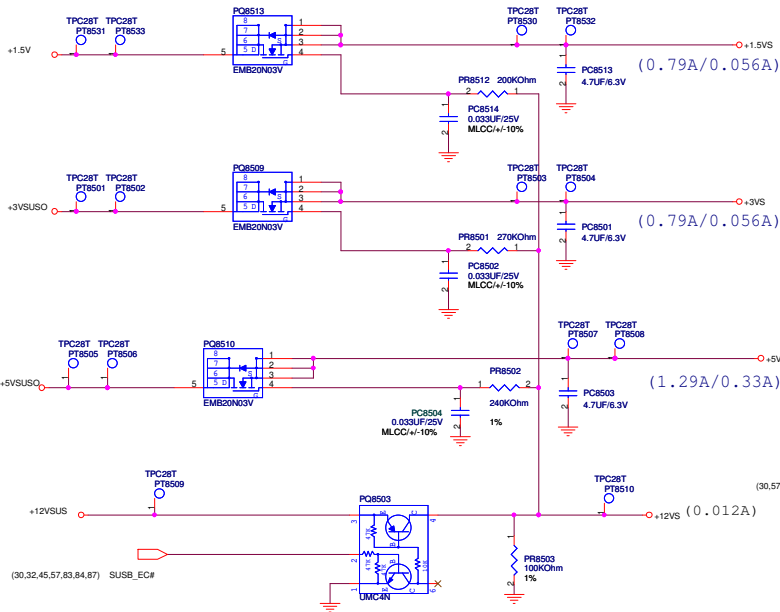
Title : Power +1.8V&+0.9V

Engineer:

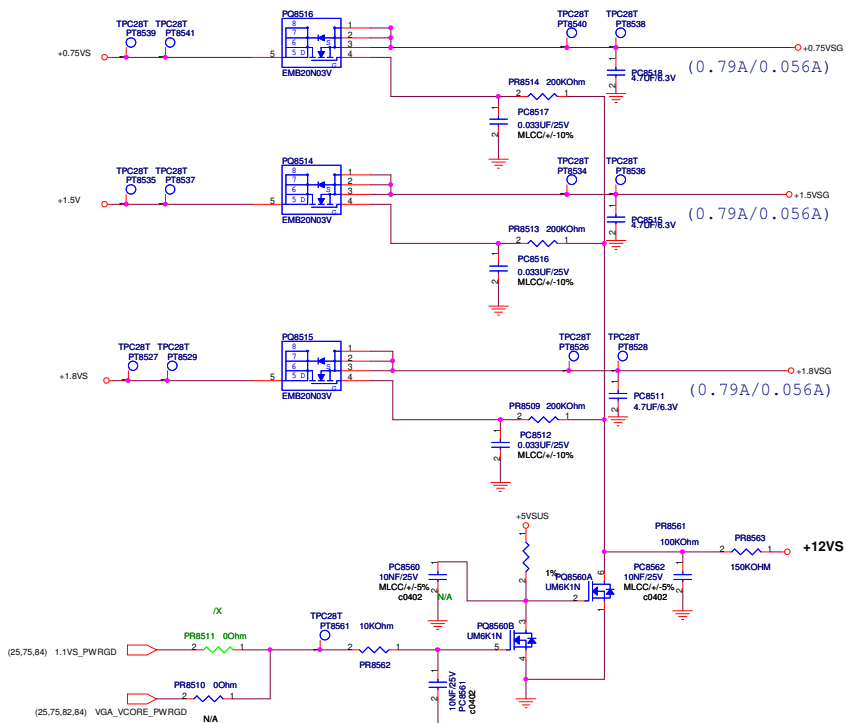
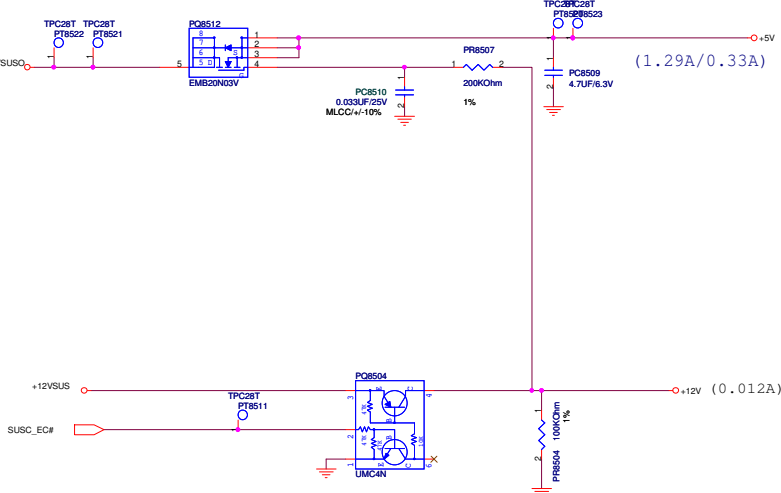
Rev 1.0

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SUSB#_PWR POWER




SUSC#_PWR POWER





<Variant Name>

**ASUS**

Title : Power_good_detector

ASUSTek COMPUTER INC

Engineer:

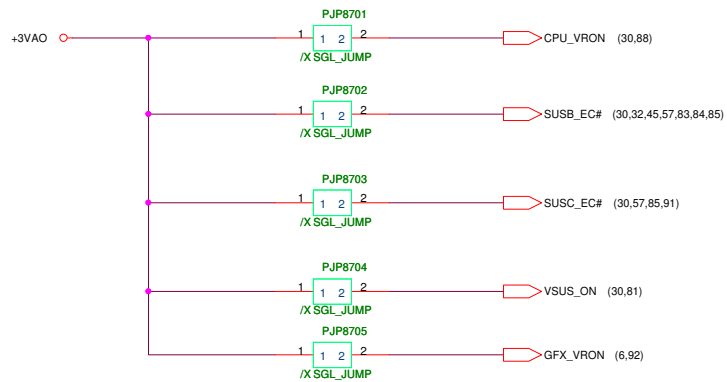
Size
Custom

Project Name


Rev
1.0

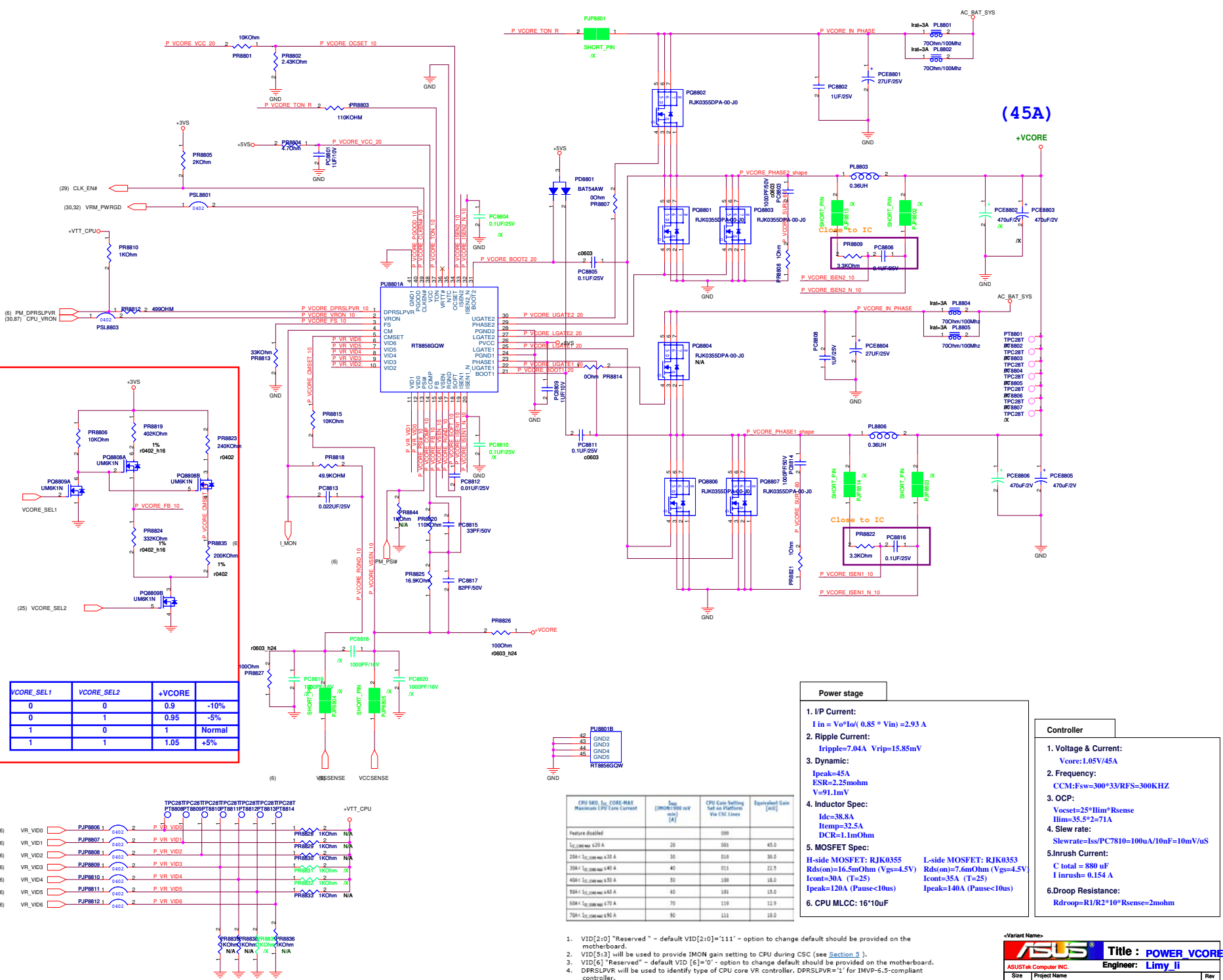
Date: Thursday, November 12, 2009

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<Variant Name>

		Title : Power_for_test	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom			1.0
Date: Thursday, November 12, 2009		Sheet	87 of 1



Power stage

- I/P Current:
 $I_{in} = V_o \cdot I_o / (0.85 \cdot V_{in}) = 2.93 \text{ A}$
- Ripple Current:
 $I_{ripple} = 7.04 \text{ A}$ $V_{ripple} = 15.85 \text{ mV}$
- Dynamic:
 $I_{peak} = 45 \text{ A}$
 $ESR = 2.25 \text{ mohm}$
 $V = 91 \text{ mV}$
- Inductor Spec:
H-side MOSFET: RJK0355
 $R_{ds(on)} = 16.5 \text{ mOhm}$ ($V_{gs} = 4.5 \text{ V}$)
 $I_{cont} = 30 \text{ A}$ ($T = 25$)
 $I_{peak} = 120 \text{ A}$ (Pause < 10us)
- MOSFET Spec:
L-side MOSFET: RJK0353
 $R_{ds(on)} = 7.6 \text{ mOhm}$ ($V_{gs} = 4.5 \text{ V}$)
 $I_{cont} = 35 \text{ A}$ ($T = 25$)
 $I_{peak} = 140 \text{ A}$ (Pause < 10us)
- CPU MLCC: 16*10uF

Controller

- Voltage & Current:
 $V_{core} = 1.05 \text{ V} / 45 \text{ A}$
- Frequency:
 $CCM: F_{sw} = 300 \cdot 33 / R_{FS} = 300 \text{ KHZ}$
- OCP:
 $V_{ocst} = 25 \cdot I_{lim} \cdot R_{sense}$
 $I_{lim} = 35.5 \cdot 2 = 71 \text{ A}$
- Slew rate:
 $Slew_{rate} = I_{ss} / PC7810 = 100 \mu\text{A} / 10 \text{ nF} = 10 \text{ mV/uS}$
- Inrush Current:
 $C_{total} = 880 \text{ uF}$
 $I_{inrush} = 0.154 \text{ A}$
- Droop Resistance:
 $R_{droop} = R1 / R2 \cdot 10 \cdot R_{sense} = 2 \text{ mohm}$

CPU SVID	I _{core} MAX	Step	CPU Core Settings	Equivalent Gain
Maximum CPU Core Current		(IMON:VDD uV mV)	Set on Platform Via CSC Lines	[mV]
Feature disabled			000	
25A < I _{core} max < 30 A		20	001	45.0
30A < I _{core} max < 35 A		30	010	36.0
35A < I _{core} max < 40 A		40	011	22.5
40A < I _{core} max < 50 A		50	100	18.0
50A < I _{core} max < 60 A		60	101	15.0
60A < I _{core} max < 70 A		70	110	12.0
70A < I _{core} max < 80 A		80	111	10.0

- VID[2:0] "Reserved" - default VID[2:0]="111" - option to change default should be provided on the motherboard.
- VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
- VID[6] "Reserved" - default VID [6] = "0" - option to change default should be provided on the motherboard.
- DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR = '1' for IMVP-5.5-compliant controller.
- PSI# - "Reserved" - default PSI# = "0" - option to change default should be provided on the motherboard.

<Variant Name>


ASUS Title : POWER_VCORE

ASUSTek Computer INC. Engineer: Limy li

Size	Project Name	Rev
Custom	K82	1.0
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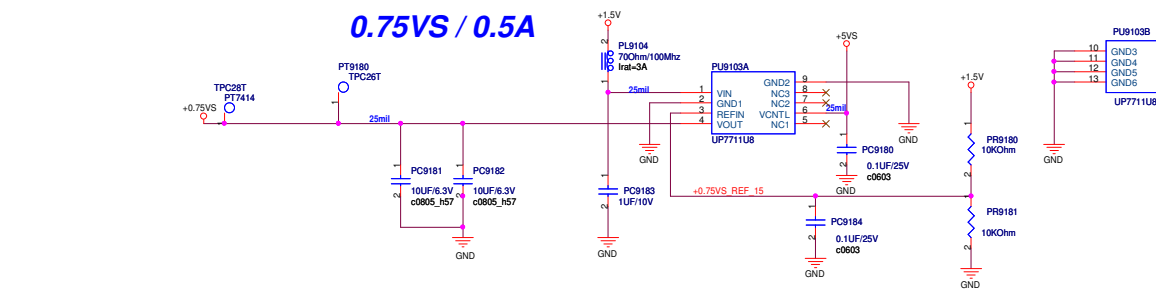
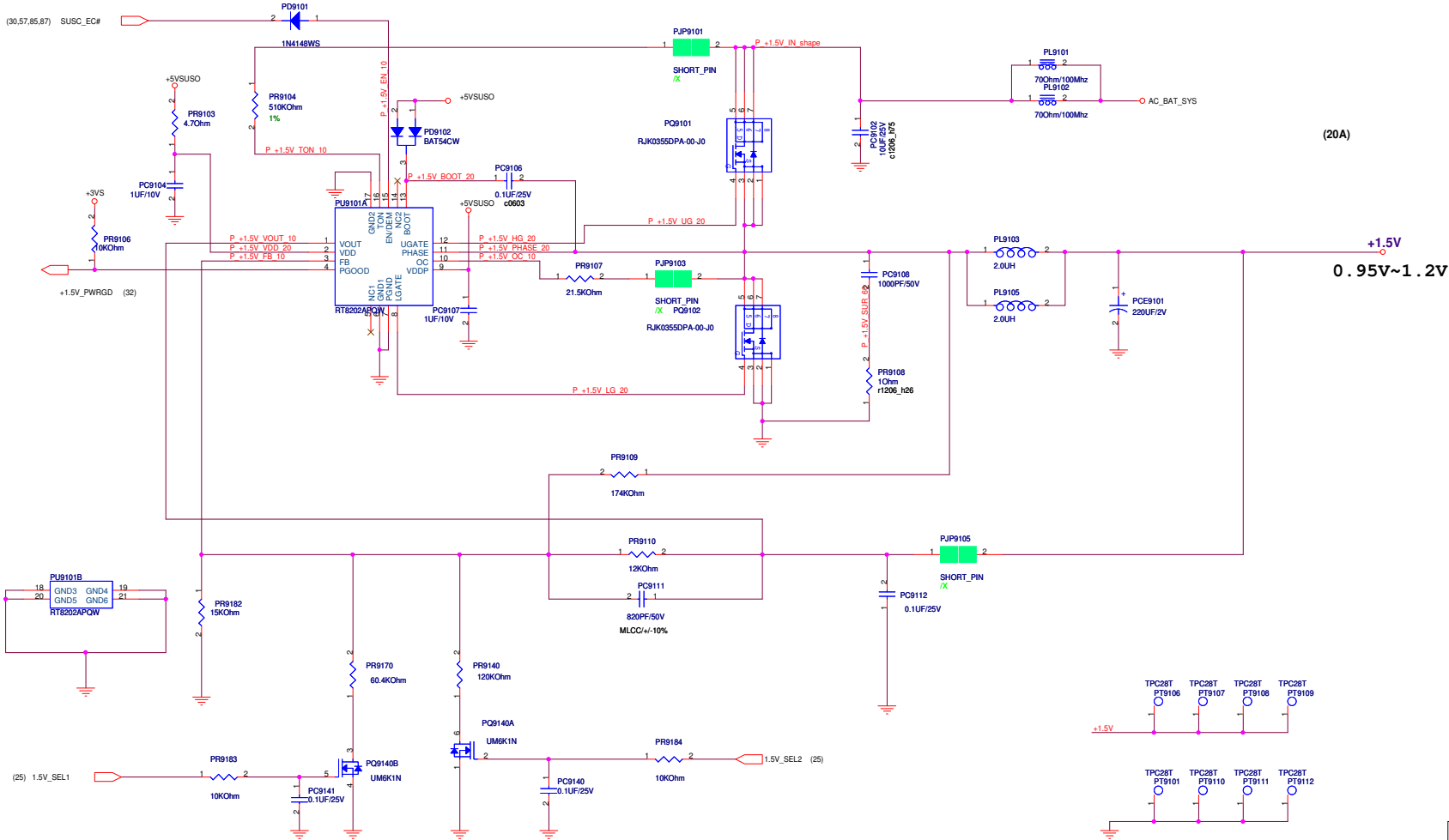
<Variant Name>

**Title : Power_Charger**

ASUSTek Computer INC.**Engineer: Lily_Ii**

Size	Project Name	Rev
A3	F83T	2.1G

Date: Thursday, November 12, 2009Sheet 90 of 1



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

Controller

1. Voltage & Current:
+1.2VSUS: 16A

2. Frequency:
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHz

3. OCP:
Set PR8107=21.5kohm
Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:
Soft-Star duration is 1.35ms

5. Inrush Current:
C total =220uF
I inrush=0.163A

Power stage

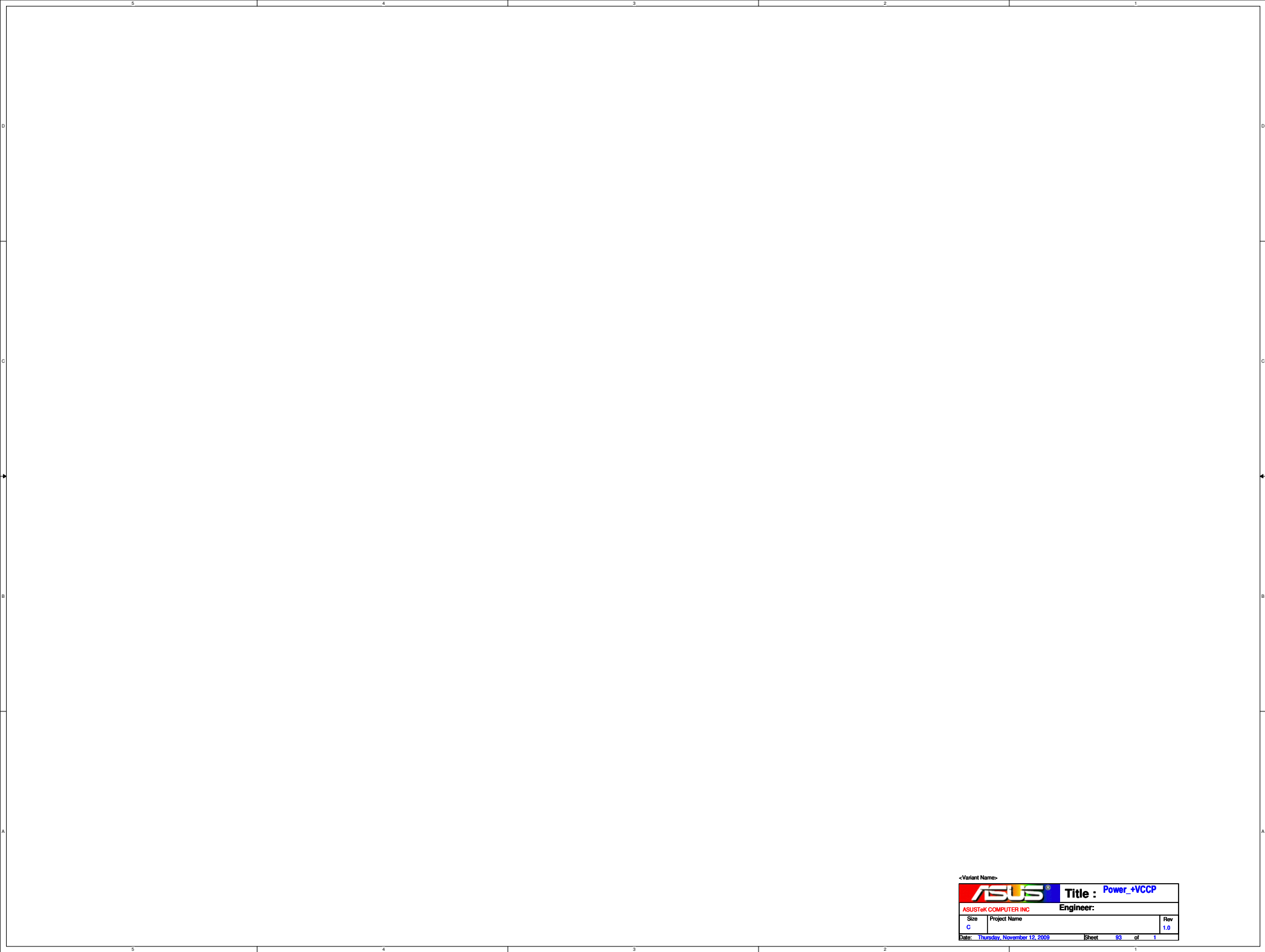
1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.85A$

2. Ripple Current:
Ripple=3.74A


3. ripple voltage:
 $I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 2.07A$
DCR=3.3mohm
V=6.831mV

4. Inductor Spec:
Isat=25A
Idc=15.5A
DCR=5.5mohm

5. MOSFET Spec:
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)



<Variant Name>



Title : Power_+VCCP

ASUSTek COMPUTER INC

Engineer:

Size

C

Project Name

Rev

1.0

Date: Thursday, November 12, 2009

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5

4

3

2

1


D

C

B

A

<Variant Name>

		Title : Power_+VCCP	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A3			1.0
Date: Thursday, November 12, 2009		Sheet	94 of 1

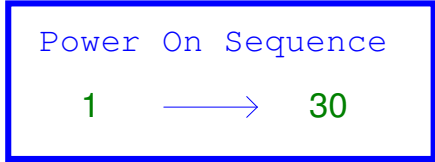
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3

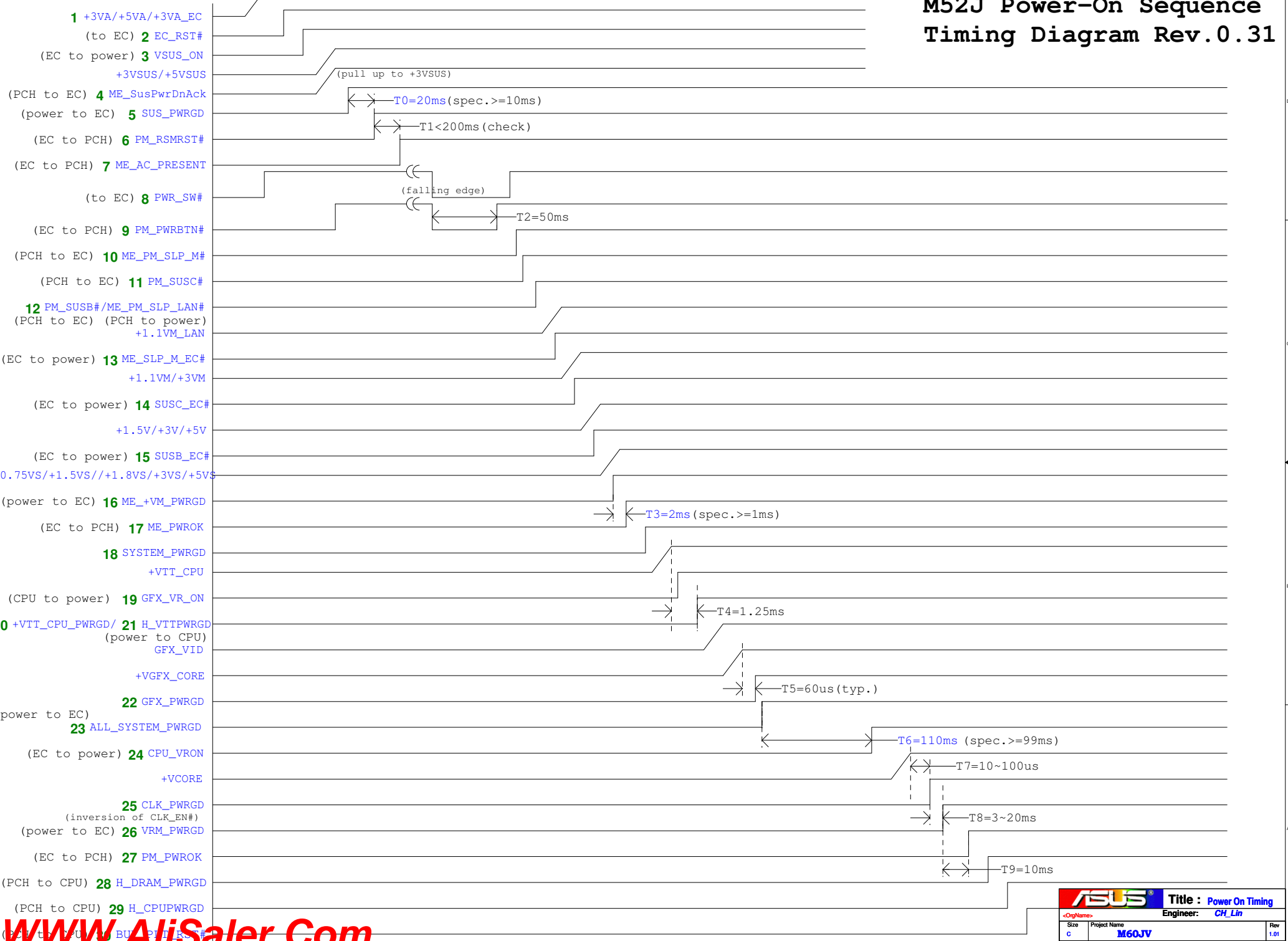
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1



AC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31



WWW.AliSaler.Com

DC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31

